To: John Schafer (and Robert Nelly)

I find these two potent applications strangely familiar itention to Fig. G of Pay care ful attention to Fig. G of "VARIABLE PLYEL DEPTH ... Compared to the diagram on page 7 of R. Nally's Alpine video proposal.

The Alpine proposal is from 9-10-93. The patent application was filed 4 27-94. Note the name VIad Bril as inventor Note the lack of R. Nally.

Any questions?



Regards, Dove Keene

Cirrus Confidential
Business Information

CL 4897

October 1992.

Frame Buffer Control

3 1 3

FIFO E

FUFOC FIFOB FIFOA

2 113

Heat briefless Use

Hoss A Control

¥ 5.8 2.8

E []]3

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Frage Outle Outle

3 II

9

Pixel Semiconductor

23

Digital Video Processor

OVERVIEW

conferencing, animation, and video capture for scaling with Video Signal Processors dedicated to compressing and decompressing video data a powerful, cost-effective solution on the desktop The CL. PX2070 Digital Video Processor provides for computer graphics and imaging. The CL-PX2070 can be used in presentations, video telesheams.

(cout next page)

Video Teleconferencing Interactive Education Systems Video EditingVideo Authoring

APPLICATIONS

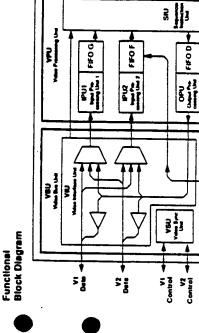
Presentation

- **FEATURES**

Supports up to three simultaneous video data

- I Video scaling
- I Complete Frame Buffer control
 I interfaces to CODECs, decoders, encoders
 I integrated ISA, MCA, and host bus interface
 - Supports both YCbCr and RGB formats 1/2 - 8 Mbytes of Frame Buffer memory

(conf. next page)



CL-PX2070 Video Processor



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A Carus Lagic Company Pixel Semiconductor

FEATURES (cont)

- Video stream formal conversion Color space conversion
- Supports up to eight simultaneous object

iem. The unit supports high speed DMA transfers of graphic or video data between the host system and the Frame Butter through direct access to

The HIU interfaces the CL PX2070 to the host sys-

HIU: Host Interface Unit

FIFOs in the Video Processing Unit, and prowdes

access to the CL-PX2070 control registers.

VBU: Video Bue Until

The VBU manages the flow of video and graphic steams between the CL-PX2070 and up to three

- Programmable, triple-channel LUT RAM
- Prescribing, zoom, and windowing Graphic and bit-mapped stream support Programmable sync steve on master When used with the Ct. PXXO'D MediaDAC!** Smalanous video and graphics daplay
- Four simultaneous, overlapping (occluded) display
 - 1024 s 768 dapley at 85 tel: Zooms born 1s to 256s

OVERVIEW (cont.)

the Frame Buffer memory management, arithmetic and logical processing, a programmable host system bus interface, flexible mainstream video dalla The CL:PX2070 extends the real time video scalng leatures of the CL-PX0070 VWG by combining path, and windowing control for multiple simultaneous video data streams.

The Ct. PX2070 has four major functional units.

- HIU Host Interface Unit
- VBU. Video Bus Unit
- VPU: Video Processing Unit RFU Reterence Frame Unit

independent devices (including the host system). Il also provides a data path between the CL-PX2070 and the host system for bidirectional graphic streams through the HIU.

Each can be configured as input only, output

Video ports V1 and V2 have the following characterisbos

eo I/O ports, and contains two subunits -- VIU and

The VBU provides two independent, real-time vid.

- only, or pixel or field duplexed I/O;
- Either port can use the sync generator provid-Each provides programmable sync polarity; ed by the CL PX2070;
- -- 16 bit 4.2.2 YCbCr, 12-bit 4:1:1 YCbCr, 16-Each supports the following formats:
 - 16 bit YCbCr, 16 bit RGB, 8 bit RGB (outbit RGB, 8 bit RGB (input).

Vidro Processor

CL-PX2070

CL-PX2070 Video Processor V2 controls the video stream data flow bo-tween the CL-PX2070 and typical CODEC de-

internal video streams through the video ports to all external devices. It specifies The VIU (Video Interface Unit) controls the flow of

the source and direction of video stream and sync control inputs;

=

- the Field-toggling Mode and field tD signals;
 - the watchdog timer feature.

The VSU (Video Sync Unit) implements identical, independent reference signals for each wdeo port:

- Vertical sync specifies the beginning of a lield or fraise.
- Horizontal sync specifies the beginning of a
- Horizontal/composite blanking specifies the horizontal/composite blanking interval.

ity for each of these signals. Two VIU master con-trol registers provide matching fields that specify input and output sync modes. FIFO D can send to. Each video port independently controls sync polarand FIFO F can receive from, the HttU directly.

VPU: Video Processing Unit

rectional real-time video streams and a single ex-ternal, bidirectional host video or graphic data Il can simultaneously process two external, bidi The VPU provides field oriented video processing

As shown in the functional block diagram on the cover, the VPU has five subunits: the IPU1, IPU2, OPU, ALU, and SIU.

age in the Frame Butter, then outputs the prepared The IPU1 (Input Processor Unit 1) prepares an instream to the Frame Buffer Data Bus, its video proput wdeo stream for ALU processing and/or stor cessing features include:

CL PX2070 mierlaces with the

processor bus

ž

Ct. PX2070 signals support the required host system address/ data impleading, and provide bidirectional buffering of the hos

CL PX2070 interfaces with the host system interface bus

Local Hardware Interface

MCA Bus Interface

ISA Bus Interface

- YCbCr and RGB input stream format conver
- color space conversion.

The host system provides the decoded chip select signal for

CI, PX2070 internally decodes the bus address during system I/O

system data bus

use with register select input

signals 8

DMA through indexed port or

ž

DMA through VO port

)MA

- programmable data tagging.
- three channel lookup table operations.
 - horizontal prescaling.
- window clipping.
- horizontal and vertical scaling, and

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A Circus topic Company

output stream format conversion.

The IPU2 (Input Processor Unit 2) provides pres caling and windowing. The OPU (Output Processing Unit) provides room.

mai, operand source selection, lagging operation selection, and arithmetic or logical operation for both held times. The ALU can process up to three smultaneous video streams input through its performs logical and tagging operations for RGB and B bit pseudo color streams. The ALU also per forms antimetic, logical, and tagging operations for YCbCr streams its registers control stream for The ALU (Anthmetic Logic Unit), shown below window chipping, and output-format functions F08

of multiple, simultaneous data streams between The SIU (Sequencer Instruction (Init) is a special purpose microcontroller that coordinates the flow the IPU1, IPU2, OPU, ALU, and OBU

cal sync pulses for each held and executing one of two different instruction sequences. The mainer in which it executes these instructions causes multitaced-video data, distinguishing between the verti The SIU is lield based when processing inter ple stream flows to appear concurrent

RFU: Reference Frame Unit

The RFU provides simultaneous access to digitit object butters and four display wintows. It has three subunits — OBU, DWU, and MMU

programmed to operate undeprindently. Object buffers may also be placed anywhere within this raster directions, FIFO association, chrominanci The OBU (Object Buffer Unit) allows each object buffer to be locked to either video source, or to be Imearly-addressable Frame Buffer OBU Registers specify the size, location, operating mode, X and Y and luminance channel masking, and output deci

play window to be any size or location. When used The DWU (Display Window Unit) allows each dis with the CL PX2080, display windows can overlap mation for each object buffer

the Frame Butter control interface for up to H The MMU (Memory Managimient Unit) provides: Mbyles of DRAM or VHAM

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PALL IMPRANT DATA SHEET

PRELEMBARY DATA SHEET

ATI01914



CONVENTIONS, ABBREVIATIONS, AND TRADEMARKS.....

Processor Interface — Local Hardware Interface Mode

Graphics Overlay Interface

Video Port 2 Intertace Frame Buller Intertace Video Port 1 Interface

Processor Interface — MCA Bus Mode

Processor Interface -- ISA Bus Mode

DETAILED SIGNAL DESCRIPTIONS.

Pin Assignment Table

PIN INFORMATION....

Pin Diagrams

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C1.-PX2070 Video Processor

Video Processor CL-PX2070



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		333	IP ID Inc	PLIZ Inou! Processor Unit 2	ş
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			-		4.3
			3 3 3 2	II'U2 Window Chpping Unit	6
4			3333	IPU2 Interrupt Request Unit	è
		114	ALU An	ALL! Antimetic and Look Unit	5
		•	1341	Operand Selection	3
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			3346	Special a-Mined Y Scaling Mode	8 3
		3 2 5	Q 0 0	OPU Output Processor Und	3
			1366	Output Format Converter	3
			1152	2 1 X Zoom Uml	5
			3353	OPU Window Cloping Unit	9
	7	1130	Reference	Reference Frame that	2
	,			Cold Ower Bullet Ind	2
		•	3	Obj Deserve Medes	=
				COD Character Modes	. 4
		342	Interup	Interrupt Request Unit	2 :
		343	OWL O	DWU Display Window Unit	?
		7 + 0	MMC	MMU Memory Management Unit	ę.
		ı	3441	3 4 4 1 Frame Buffer Architecture	9
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÷	5				=
	7	3	tosi Interis	HILL Host Interface Unit - Registers	5 6
		=	ES CS	HIU CSU Configuration Setup (Read Only)	à :
		412	£ 08	HIU DBG. Debug Control (Write Only)	8
		413	HILDR	HIL DRD Debug Read (Read Only)	Z
•		•	00	HILL OCS Operation Control/Status (Read/Write)	82
2			-	HILL IND. Intercool Request (Read Only)	9
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	7	38	Video Bus	VBU Video Bus Unit — Registers	₹ :
		421	VIC V	VIU Video Interface Unit	5
			4211	VIU MCRp Master Control	5
			4212	VIU DPCI Datapath Contol	6
			4213	VIU WOT Watchdog Temer	5
		422	VSU V	VSU Video Sync Unit	8
•			4221	VSLI HSW Horizontal Sync Width	£
į				VCIT MAD Movionial Arina Delay	£
			777	TOTAL STREET STREET BOOK STREET	3
			4223	VSU HAP HONZONIZA ACINE PILEIS	6
			4224	VSU HP Montonia Pendo	ð
			4225	VSU VSW Vertical Syric Wigh	2 3
			4226	VSU VAD Vertical Active Delay	ř

0

Host System Bus Configuration

3113

Cl. PX2070'Contiguration

3 t 1 Hardware Configuration

HILL Host Interface Unit

FUNCTIONAL DESCRIPTION

Power and Ground

3114 Fort Autress Contquation Register and Frame Buffer Interface 3121 Internal Register Access Frame Buffer Configuration

312

Accessing the Frame Buffer

Girput Formal Conventer and Chrominance Interpolator ...

Color Space Converter

Input Tag Unit

Window Clipping and XY Scaler

X Prescaler LUI PAM

Accessing FIFO Control/Slatus Indicators

IPU1 Input Processor Unit 1

332

Sequencer Instruction Memory SIUs., SIM

Programming the SIU
Master Control Hegister SIU MCR

SIU Sequencer Instruction Unit

3.2.3 VSU: Video Sync Unit VPU Video Processor Unit

33

32.2.1 Video Stream and Sync Control inputs 32.2.2 Field Togging and Field ID 32.2.3 Watchdog Time

VIU Video Interface Una

Video Ports V1 and V2

VBU Video Bus Unit

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CL.-PX2070 Video Processor

CI.-PX2070 Video Proressor





		422	4227 VSU VAP Vertical Active Press	4363 OPU KEN KIND	<u> </u>
		422	4228 VSU VP Vertical Period	4364 OffU VB# V Bogin	5
•		U Video	VPU Video Processor Unit Registers	4365 OPU YEN YEND	=
	7	431 VPU		4 4 Rt U Reference Frame Unit — Registers	- 36
		-0,		44.1 OBI Obset Bullet Und	-
	432				-
		4321			=
		4322	(21) IC Instruction		?
		4323			Ξ
		, ,	ILOI TLC. FIND COURT		=
		77.		5 - 4 - 5	-
		4325	IPU1 FIR. Field Count Interrupt Request		
		4 3 2 6	IPUL I RB LUT PAM Base Address	4 4 2 1 MANU MCR: Master Control	
		4327	IPU1 LRD 1UT RAM Data	4 4 3 DWU Display Window Unit	
		4328	IPU1 MCRI Master Control	4 4 3 1 DWU MCR Display Window Master Control	=
		4329	IPUI XBrt X Bean	4 4 3 2 DWU HCR: Display Window Horizontal Control Register	=
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Imput Tag Unit.
Window Clipping and XY Scaling Control Registers.
Imput Processing Unit 2.
IPUZ 2 1 Prescue Example

IPUZ Window Choping Unit ALU Simplified Block Diagram ALU Anthmetic and Logic Unit

Possable Paths for Video Data.

Register Access

Local Hardware Interface Write Cycle.

Read Timing (Local Hardware Interface).... Local Hardware Interface UMA Cycles

Figure 3-10.

Figure 3 11

ISA and MCA Interface Address/Data Multiplexers MCA Bus Interface for Register Access Cycles.......

Detault (Local) Contiguration ISA Bus triendace for Register Access Cycles ISA Bus Interface for DMA Cycles

Figure 3.6. Figure 3.7 Fgure 3 8

Typical CL PX2070 System Interconnection

Figure 3.2

Figure 3.3 Figure 3.4

Video Prox essor CL-PX2070



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CL -P.X2070 Package Information (Expanded View)

CL. PX2070 Package Information

Figure 5.9

Write Timing (Local Hardware Interface)

MCA I/O Cycle Timing COSF DBK* Timing (MCA Bus) COSETUP* Timing (MCA Bus)

Figure 5:3 Figure 5.4

VSU Honzontal Sync Timing

VSU Vertical Sync Timing DAMA Timing (ISA Bus)

VO Temmo (ISA Bus)

Typical Frame Buffer Implementation

Display Window Frame Buffer Addressing (16 Bit)

XY Bt.1 Direction Control

Figure 3.27 Figure 3.27 Figure 3.29 Figure 3.30 Figure 3.31. Figure 3.32.

Object Buffer

Frame Buffer Addressing (32 bit) Reference Frame Allocation OPU Output Processor Unit.

The Reference Frame Unit

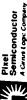
Figure 3.25

Read Timing (Local Hardware Interface). . . .

Figure 5:5. Figure 5:6. Figure 5:7

DMA Timmy (Local Hardware Interface)

Input Video Firming



Somiconductor

CL.-PX2070 Video Processor

CONVENTIONS, ABBREVIATIONS, AND TRADEMARKS

CONVENTIONS

Conventions used in this document are described in the following example:

Ropster names that contain lower case variables represent groups of registers with similar functions for example, VII.) DPC/represents both of the Datapath Contoi register. — register VII.) DPC1 (Datapath Contoi Feld 2) and register VII.) DPC2 (Datapath Contoi Feld 2). Table 4.1 on page 84 defines all variables used in this manner. VIU DPCI

ABBREVIATIONS, ACRONYMS, and MNEMONICS

Abbreviations, acconyms, and mnemonics used in this document are described in the following table:

AI U	Anthmetic and Logic Una	
CODEC	Code/Decode or Compress/decompress	Compress
מאַ	Central Processing Unit	
5	Cathode Ray Tube	
CIAG	Control Tag Multiplexer signal	
DMA	Duect Memory Access	
DHAM	Dynamic Random Access Memory	017
D.M.O	Ursplay Window Unit	
180	Frame Buffer Data	
FIFO	First In First Out	
ISA	Industry Standard Architecture	
Q	Input / Output	
LSA	Linear Start Address	
JPEG	Joint Photographic Export Group	0
188	Least Significant Byte	
Se	Least Significant bit	
בּ	Look Up Table	
MCA	Micro Charmel Architecture	AT
MMILI	Memory Management Unit	·IC
MSM	Mosi Sqinikani Byte	01914
9		8

Video Processor CL.PX2070



MSD	Most Significant bit
OPU	Output Processor Unit
OTAG	
Ē	Input Processor Unit 1
1PU2	
POFP	
PSE	
RGB	
RAM	
PF.U	
StM	
SrU	Sequencer Instruction Unit
VPU	
VRAM	
YCBCı	inarice Y Ohie
	MASD OPU OPU OPU IPUI IPUI IPUI IPUI IPUI IP

TRADEMARKS

Trademarks used in this document are described in the following table:

MediaDAC¹⁴⁶ is a trademark of Pixel Semiconductor, Inc

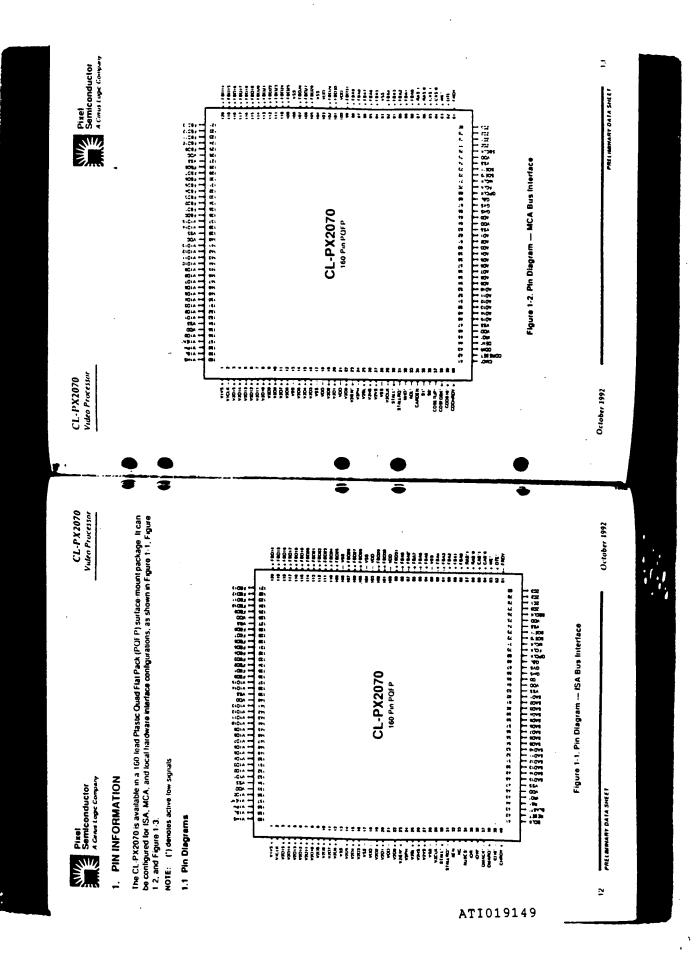
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C.L.P.X2070 Video Processor

CL-PX2070

Video Processor

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1.2 Pin Assignment Table

The following conventions are used in the pin assignment table

- active low signal I - input

O - output

VO - inputouput

PWR - power

TII. - the pact has standard TII. input threshold and output fevels

OD - open drain, TII. inputs

4 - 4-mA sink and 2-mA source drive capability

24 - 24-mA sink and 6 mA source drive capability

NA - not applicable

| COLUMN | C

															in fileston	•
FUNCTION		Address/Data Bus	Data Buffer Enable	Data Buffer Direction	I/O Read	LO Write	Address Enable	UMA Request	DMA Actinowledge	Interrupt Request	Channel Ready	16 Det VO Cycle	Bus Clock	Reset	No Connect (must be inft feature)	Auxiliary Chip Select
CELL	30E	T. E.	111.0	111.8	=	Ē	ĭ	111.4	=	111.4	111 24	111.24	Ξ	1	¥Ž	ĭ
TYPE	PROCESSOR INTERFACE - ISA BUS MODE	3	8	8	-	-	-	0	-	0	8	90	-	-	Ž	
PIN	A INTERFACE	48.62, 65	=	\$	35	8	8	8	37	\$	ę	88	Ŧ	45	33	2
NAME	PROCESSO	SAD(15 0)	N30	DOIR	HOI	MQ	AEN	DMARO	DMACK.	Ĕ.	CHRDY	.9101	BCLK	RESET	¥	AUXCS.

CL-PX2070 160 Pm PQFP

50	48.62, 65	3	ř	Address/Data Bus
	7	8	11.8	Data Nuller Enable
DDIR	+	8	111.8	Data Buller Direction
	38	-	=	Status 1
.os	98	-	E	Status 0
DEN	75	-	11	Card Enable
	35	-	Ē	Memory or VO Cycle
CDSFUBK.	8	0	111.4	Card Select Feedback
EIG.	37	-	=	Card Setup
	\$	0	11.4	Interrupt flequest
нпру	9	9	111.24	Channel Ready
.916	28	90	111,24	Card Data Size
_	ŧ	-	Ξ	Command
CDRESET	45	-	Ξ	fleset
Ø	33	-	=	Astronom Care to

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Figure 1-3. Pin Diagram — Local Hardware Interface

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PROCESSOR INTERFACE — LOCAL HARDWARE INTERFACE MODE

DI15 01 46 62, 65 LO TIL, 4 Date Bure

HS[31] 34 33, 44 I III. Regular Saleci

BLAST 35 1 III. 4 Burel Last

ION' 35 I III. 4 DATA REGULAST

DIAARIO' 38 O TIL, 4 DATA REGULAR

DIAARIO' 39 O TIL, 4 DATA REGULAR

HINO ' 45 O TIL, 4 DATA REGULAR

FIND ' 40 O TIL, 4 DATA REGULAR

FIND ' 40 O TIL, 4 INTERFACE MODE

HIND ' 40 O TIL, 4 INTERFACE MODE

HIND ' 40 O TIL, 4 INTERFACE MODE

HISTORY 40 O TIL, 4 INTERFA

Vencal Syric Honzonial Syric Honzonial/Composite Banking Phase Input Enable

EEEEE

333-0

137 138. 141 153, 156 160 159 158

VIVS VIHS VIPH VIPH

Video Data Clock Video Data Bus

_ 2

VICLE VIDI15 0J

VIDE O PORT 1 INTERFACE

Pixel Clock Vertical Sync Honzontal Sync Blanking

EEEE

GRAPHICS OVERLAY INTERFACE GPCLK 69 I GVS 67 I GHS 66 I

Ventcal Sync Horizontal Sync Horizontal/Composie Blanking Phase Input Enable Stall Request

555-0-0

VZVS VZHS VZPH VZPH VZPH STALLHO: STALL

Video Data Clock Video Data Bus

ΞË

_ 8

VIDEO PORT 2 INTERFACE V2CLK 29 V2D[15 0] 3 12, 14 16

CL-PX2070 Video Processor

FUNCTION ROAD

CL.-PX2070 Video Processor

Semiconductor

NAME	PIN	TYPE	CELL	FUNCTION (com)
FRAME BUF	FRAME BUFFER INTERFACE			
FB0/31.0J	99, 101 102,	δ	TIL, 4	Data Bus
	109 125.			
FBA(9 0)	98 94, 92 88	0	111,8	Address thus
PASI 0	97 86	0	11.6	Row Address Strobes
CAS[1 0].	95 84	0	11.8	Column Address Strobes
WE.	93	0	111, 12	Write Enable
01E	85	0	TIL, 12	Data Transfer Ernable
FRDY		-	Ξ	FIFO Heady
SC(3 0)	60 //	0	7 T	Zoom Control Bus
SBCLK	92	0	11.8	Senal Bus Clock
SOEI1 01.	23 72	0		VRAM Senal Port Output Enable
MCLK		-	=	Memory Clock
FCLK	8	0	11.8	FIFO Write Clock
POWER				
001	18, 21, 46, 64, PWH	PWH	4	• 5 VDC for Digital Logic and Interface Buffers
	75, 100, 103,			•
	126, 140, 155			
vss	13, 17, 28, 47, PWIR	₽₩I	4	Ground for Digital Logic and Interface Buffers
	63, 74, 93,			
	104, 108, 127,			
	139, 154			

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2. DETAILED SIGNAL DESCRIPTIONS

2.1 Processor interface — ISA Bus Mode

Signel	Pin	Type	Cell	Function
la si lavs	48 62. 65	2	į	Addresa/Data Bus: Borrectional, multiplexed address/data bus Ptal transfers video data between the host system and the CL-PX/2010.
DEN.	.	8	111.8	Date Buffer Enable: When pufled low, enables the host data bus buffer
HIGO	ç	8	111.8	Deta Buffer Direction: Specifies the draction of data flow When high, the host system is writing data to SAD(15 q; when low, the host system is careful data from Salvie or
EQ	35	-	Ē	VO Reed: Specifies an I/O read cycle
ΩW.	æ	-	Ξ	VO Write: Specifies an tro water conta
AEN	25	-	Ē	Address Enable: Standar ma - Date
DIMARIO	8	0	11.4	DMA Request: Specifies that the CL - PX2070 is requesting a DMA transfer.
DMACK.	3/	 !-	ĮΞ	DMA Acknowledge: Specifies that the host system is ready to perform a DMA tracetar
<u>0</u>	\$	0	E.	Interrupt Request: Specifies that the CL-PX2070 is requesting
CHHDY	Q	90	111, 24	Channel Ready, When pulled the species that the CL PX2070 is not ready to complete the curent host access cycle. The CL PX2070 is not ready to complete the curent host access cycle should be controlled to indicate that the current host access cycle should be controlled.
.9101	33	00	TH. 24	16-bit VC Cycle: Species that the Ct. PX2070 is able to respond
BCLK	÷		=	Bus Clock: Clock included to synchronize access between the host stream and the Clocks.
RESET	42	_	É	Reset: Causes the CL-PX20/0 to cease all activity and perform a hardware lesse.
Ş	33	N/A	¥ 2	No Comment figures has to a march
AUXCS.	*			Aurillery Chip Select: When programmed for AuriSA Mode, pri- mary and secondary addresses are ignored AUXCS' and SAQ1 11 select specific reasters.

CL-PX2070 Video Processor

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CL.-PX2070 Video Processor

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2.2 Processor Interface -- MCA Bus Mode

Signal Pin Type Cell Function

A0(15.0)	48 62. 65	8	III. 4		ata Bus	Address/Data Bus; Undrectional, multiplexed address/data bus that transfers video data between the host system and the CL. PX2070
OEN.	3	8	111.6		r Enable	Deta Buller Enable: When pulled low, enables the host dula bus buller
DOIR	₽	8	TIL. 8	i	Direction St. System	Data Buffer Direction: Specifies the direction of duta flow. When high, the host system is writing data to SAIX is by, when low the host system is reading duta from SAIX is by.
S1.	SC	-	E	Status 1: Used with MAR (see table under MAO*)	sed with	Status 1: Used with MAO' and SO' to specify the current bus cycle (see table under MAO')
.0S	æ	-	Ĕ	Status 0: Used with Mrit (see table under MriO*)	sed with in	Status 0: Used with MAO' and S1' to specify the current bus cycle (see table under MAIO')
CARDEN	ň	-	E	Cerd Enabl	e: Specif	Card Enable: Specifies that the data on bus A()(15 H) is valid
.Our	35	-	Ĕ	Memory or IV	1/0 Cycl	Memory or UO Cycle: Used with St. and St. to specify the cure of bus cycle
				.03 6		:
				•	۰ .	Heserved
					- 0	VO Wile
				-	-	Huaciive
				•	•	Neserved
				•	-	Mernory Write
				- ·	0	Memory Read
				-	-	maciwe
CDSF DBK.	8	0	T. 4	Card Select	Feedbec	Card Select Feedback: Specifies that the Ct. PX20/0 has the put
				ed the curren drive CDSFD low)	BK tow	ed the current address and status inputs. The CL 1920 to obes not drive CDSF DBK* fow during the configuration period (CDSE TUP* fow).
COSE TUP	37		Ĕ	Card Setup: S figuration (POS adapter (The a forming an VO: 101, and 102.)	Specifical Specifical Specifical adapter Tread cy	Card State; Specifies that the host system is accessing the configuration (POS; programmate option select) registers of the MCA adapter (The adapter (The adapter (The adapter (The adapter)) and configuration data is obtained by beindoming an VO read cycle to the CL PX20/0 it contains POS; 100:101; and 102.)
190.	\$	0	11.4	Interrupt Request: Specifies service from the host system	quest: Sg	Interrupt Request: Specifies that the Ct. P X20/0 is requesting service from the host system.
сосниру	ę	8	11.24	Channel Ready: When pulled towns is not ready to complete the curter Ct. PX2070 releases CDCHIHIPY is access cycle should be completed	dy: When completed complet	Channel Ready: When pulled low, specifies that the CL 1720/0 is not ready to complete the current host access cycle. The CL PX20/0 releases CDCHIHITY to indicate that the current host access cycle should be completed.

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CL-PX2070 Video Processor



Signel Pin Type Cell Function (cont.)

Signel	됩	Type	Ce	Pin Type Cell Function (cont)
CUDS16" 39 OU 111,24 C	ይ	3	111.24	111, 24 Card Data Stae: Specifies that the CI PX2010 is able to respond as a 16 bit VO data device for both read and write cycles.
CMD.	Ŧ	-	Ξ	Command: Specifies that valid data is on bus AU) 15 0j during a wile cycle, and that the CL PX20/0 should place valid data on the bus during a read cycle
CDINE SE I 42	45	42 1 111.	=	Reset: Causes the Ct. PX20 /0 to cease at activity and perform a hardware reset.
ADK.	g	-	i	Address Letch: Used to demulipte in the address from bus AUTS 01, and status from signals M/O°. Sit, and SO°. The address and status must be valid during the LOW to HIGH transision.

2.3 Processor interface — Local Hardware Interface Mode

O(15 0) 48 65 RS(3 1) 34	ĺ			
	46 62. 65	8	H. 4	Deta Bus: Bidirectional data bus that banslers video data between the host system and the Ct. P X2070
*	4 33	_	Ĕ	Register Select: Specify the register address during a host access
BLASI 43		0	111.4	Burst Last: Specifies the last cycle of a DMA transfer.
10R' 35		<u> </u> _	Ē	VO Read Cycle Specifies an VO read cycle
KOW" 36		_	11.	VO Write Cycle. Specifies an I/O write cycle
cs. 32		_	Ĕ	Chip Select Specifies that the host system is accessing the CL-Px2070.
DMARG. 38		0	1	DMA Request: Specifies that the CL-PX2070 is requesting a DMA transfer.
UMACK' 37		_	Ē	DMA Achnowledge: Specifies that the host system is ready to perform a DMA transfer
190' 45		0	11r. 4	Interrupt Request: Specifies that the CL.PX2070 is requesting service from the host system
CHRDY: 40		go	711, 24	Channel Ready: When asserted, indicates that the CL PX2070 is not ready to complete the current host access cycle. The CL-PX2070 releases CHRIDY to indicate that the current host access cycle should be completed.
PCIK 41		_	=	Processor Clock: This impul clock is used to synchronize the flow of data on bus U(15 0) during UMA data transfers.

				Cease all activity and perform a hardware reset
Ş	æ	¥	₹2	No Connect: (must be toff foating)
.4 Grapl	hics Ove	· 2.4 Graphics Overlay Interface	1ace	-
Signet	P.	Туре	Type Cell	Function
GPCLK	2	-	Ę	Pixel Clock: Clocks display output pixel data from the graphics controller
GVS	3	_	Ĕ	Vertical Sync: Identiles the start of the vertical sync interval. A vertical sync pulse is generated once every head time for interlaced data, and once every frame time for non interlaced data. Its potarriy can be specified as either active fugh or active tow.
GHS	8	-	E	Horizontal Sync, identifies the start of the horizontal sync merval. A horizontal sync pulse is generated once to each input line. Its potanty can be specified as either active high or active tow.
1 50	8	-	111	Blanking identities the transing interval its polarity can be specified as either active high or active low.

2.5 Video Port 1 Interface

Pin Type Cell Function	Video Data Clock: Cloc	Video Data Bus: E between the CL P)	TTL, 4 Vertical Sync: identifies the start of the vehiclal sync interval A vehiclal sync pulse is generated once every held time for intertaced data, and once every frame time for inon interfaced data. If can'be specified as active-high or active-low.	# Ca	. 4 Moisonist Composie Blanhing Identiles the Danhing afferval it can be specified as active high or active tow
5	Ę	11.4	Į.	TH. 4	¥.
Type	-	<u>s</u>	ç	Š	S.
ş	7	156. 153 141. 138 137	-	9	159
Signaf	VICLK	V:0(15.0)	SAIN	SHIA	i

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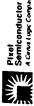
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Video Processor C1.-PX2070

2.7 Frame Buffer Interface



Signal Pin Type Cell Function (cont.)	(pool
- 951	
lo si hi i A sno	o data qu
₹ .	111. 4 Input Enable: Specifies that the CL PX2070 is not driving bus VID(15.0) VIEW can be used as a traite control by an external buffer connected to bus VID(15.0)

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Signat	e G	Type	3	Function
V2CI K	8	-	Ĕ	Video Data Clock: Clocks bidwectional video data on bus V2Uj 15 oj
v2U15 0	3.12. 14.16. 22.00.	3	11.4	Video Date Bus: Translets wdeo data between the CL PX2070 and an ellernal device
vzvs	12	3	=	Vertical Sync: identifies the start of the ventcal sync interval. A ventical sync pusers generated once every held time for interfaced data, and once every fame time time to non-interfaced data. V2VS can be specified as active high or active-low.
V2HS	56	ð	÷ :	Horizonial Sync: Identifies the start of the horizonial sync enerval. V211S can be specified as either active high or active-low.
VZBI	\$2	9	₹	Horizona V.Composite Blanking: Identifies the blanking interval V28t can be specified as active high or active low
У2Р Н	54	-	Ĕ	Phase: Controls data qualification and duplexing of video-data on bus V20(15.0)
VZIEN.	C2	0	11L. 4	Input Enable: Specifes that the CL P X2070 is not driving bus V20(15 0) V21EW can be used as a bristate control by an external buffer connected to bus V20(15 0)
STALL RO.	ñ	-	Ë	Staff Request: Requests that the current transfer of video data on bus V2[X i S 0] be suspended
STALL.	e 8	0	11.4	Stati: Specifies that the CL:PX2070 has suspended transferring date on bus V2D(15.0)

NOTE: Video input data mapping to the video data bus depends on the input-data format. See Section 3.3.2.1 for detailed information.

Address Burs. Multipliced output bus that specifies an address to the frame fluifier. The row address is valid during the Hillist to LOW transition of separals KNS[10] is used the coheren address is valid during the HIGH to LOW transition of separal CAS[10]. Row Address Strobes in situation for frame thanks to later the row address from bus FBA[9 0] during the HIGH to LOW transition. FIFO Ready: (CL PX2080 Mode) Specifies that the CL PX2080 is ready to receive senal data from the Frame fluiter into 4s injud FIL, 4 Data Bus: Ridirectional data bus that transfers duta between the CL-PX2070 and the France fluifer column address from bus FBAI9 0) during the HIGH to LOW tran FIFO Wrde Clock: (CL PX2080 Mode) Clocks send data into the CL PX2080 Column Address Strobes; Instruct the frame Buffer to lawn the VRAM Serial Port Output Enable: Cause the Frame Buffer to as sent the serial data port TTL, 12 Data Transfer Enable: Specifies a fransfer cyclo to the fruine Memory Clock: Synctronizes all Frame Buffer control signals Seriel Bus Clock: Clocks senal data from the Frame Huller Zoom Control Bus; (CL. PX2080 Mode) Specifies to the CL-PX2080 the zoom lactor to be used on the current status TTL, 12. Write Enable: Specifies a write cycle to the Frame Buller Buffer (VRAMs only) (VPAMs only) Function 11.8 ٦. ٦. TL, 8 = 0 Ē Type 136 128, WO 125 109, 107 105, 102 101, 0 0 0 0 0 0 0 0 0 98 94. 92.88 97 86 85.84 200 73 72 퉅 2 2 92 Ξ 2 FB031 0 FBA[9.0] Signal PASH 0 CASH of SOE(1 ol. 10 c/52 SBCLK MCLK FROY Ę we.

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2.8 Power and Ground

CI.-PX2070 Video Processor

Video Processor CL-PX2070



3. FUNCTIONAL DESCRIPTION

up to two external, bidirectional, real time video streams and a single external, bidirectional host video or graphic stream, and three related subsystems that perform complice interface functions. Figure 3.1 shows, a functional block diagram of the CL PX2070. The CL PX2070 contains four major functional blocks - - a core Video Processing Unit, which can prixiuss

+5 VDC for Digital Logic and Interface Buffers: Each VDD pm must be connected directly to the VDD plane

Function

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Type

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Signal <u>Ş</u>

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Ground for Digital Logic and Interface Buffera: Each VSS pm must be connected directly to the ground plane.

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13, 17, PWH 20, 47,

VSS

93.104

139, 154

140, 155

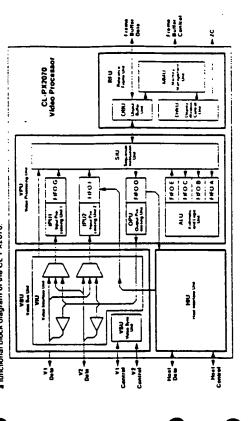


Figure 3-1. Functional Block Diagram

The Host interface Umi (HIU) is a complete host interface that can be configured for ISA Bus, MCA Bus, or local hardware interface operation. The HIU is the communication and data path between the host system and the CL. PX2070 based display system. See Section 3.1 on page 27 for authinoral information.

- The Video Bus Unit (VBU) is a highly programmable I/O path for video data. It contains two external digital video I/O ports, an internal input path from the HIU to the VPU, a sync unit, and a watchulug timer. See Section 3.2 on page 38 for additional information
- master control register, a Sequencer Instruction Unit, two Input Processor Units, air Arithmetic, arixt Logic Unit, and an Ouput Processor Unit. See Section 3.3 on page 46 for additional efformation The Video Processor Unit (VPU) provides held: or frame oriented video processing. It contains the
- tains an Object Buffer Unit, Display Window Control Unit, and Memory Management Unit. The HE to directly controls DRAM/VRAM devices, and defines up to eight graphics objects in multiple display. The Reference Frame Unit (RFU) manages the video data flow to and from the frame butter. It comwindows. The innovative use of reference frames allows display windows to be resized and movem rapidly, with little CPU or software overhead. See Section 3.4 on page 70 for additional information

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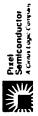
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Figure 3.2 shows the relationship of these blocks to each other, and the interconnection of the CL. PX2070

in a typical system

C.L.-P.X2070 Video Processor

Video Processor CI.-PX2070



3.1 HIU: Host Interface Unit

The HIU, shown in Figure 3.1, provides the interface between the CL. PX20/0 and the host system. It supports high speed DMA transfers of graphic or video data between the host system and the Franne Butter contains address decoding, Interface Registers, and refated functions, and provides access to the CL. PX20/0 Control Registers.

The HIU has two primary control functions:

 Register and Frame Buffer Interface. Hardware Configuration

3.1.1 Hardware Configuration

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CODEC

CUDEC

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CL.PX2070

The HIU is central to the following hardware configurations.

CL. PX2070 Configuration

Host System Bus Configuration Frame Buller Configuration

Port Address Configuration.

3.1.1.1 CL-PX2070 Configuration

The CL. PX2070 is configured during power up reset. The state of FBD/S 0) is written to the lower live bit. of Register HIU CSU at the failing edge of RESET. The FBD Signals are internally publicf up, which results in a 111 code (Local Mode) in HIU CSU (See Section 4.1.1 on page 82 for additional information.

Table 3.1 shows the HIU_CSU bit-field assignments.

Table 3-1. Register Bit Assignments — External and Default (Local) Configurations

For additional detail concerning specific CL PX2070 registers discussed in this section, refer to Section 4. NOTE: Hegister names that contain lower case variables represent groups of registers with similar functions. For example, VRL DPCI represents either or both of the Datapath Contol Registers.—Register VIL DPCI (Datapath Control Fred 1) and Register VIL DPCI (Datapath Control Fred 1) and Register VIL DPCI (Datapath Control Fred 2). Table 4-1 defines at van-

ables used in this manner

Figure 3-2. Typical CL-PX2070 System Interconnection

Function (Default Configuration)	Defaults to kocal hundware unerface
Function (External Configuration)	Host System Specifies the host system connected to Defaults to kical hardware Bus the CL PX2070 to be ISA, MCA, or local interface.
efinition	Host System Bus
HIV CSU Field	нЅВ
Signal(s) Field D	FBUIS 31 HSB

FBD(2)		Reserved		
1.087	181	Frame Buffer Type	Frame Buffer Species the Frame Buffer memory to be Defaults to VIRAM Type DRAM or VIRAM IT has be redicates the condition of FBU during testi, which is sometimes useful to apprication software If has no effect on how the trains buffer refalse functions	Defaults to VIRAM
FBU(0) PAS	PAS	Port Address Select	Port Address Specifies whether the host system should it was 1455 is not wheten it select the primary or secondary I/O local hardware interfar each address map when accessing the specified by Soquis CL PX20/0 (SQC) (SQC)	Light PAS is not active in local hardware interfar e mode. Address discorte specified by Signals. PISE II (see father 1-a).

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Esternal Configuration

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Video Processor CI.-PX2070

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3.1.1.2 Host System Bus Configuration

The HIU interfaces to two popular PC expansion buses

External configuration is always used to configure ISA and MCA systems. The CL-PX2070 selects this configuration when any of FBUIS. 3] are low. As shown in Figure 3.3, the CL PX2070 reads the configuration when any of FBUIS. 3] are low. As shown in Figure 3.3, the CL PX2070 reads the configuration and atlast from Frame Builter Data Bus Signals FBUIS. 0]. These signals are latched into the LSB of Register HTU CSU from an external instate builter at the failing edge of Signal RESET. Table 3.1 shows the bit to field mapping required for the data on these signals.

For higher performance, the CL PX2070 can also reside on the local hardware interlace Industry Standard Architecture (ISA) Bus; Micro Channel Architecture (MCA) Bus

Table 3.2 highlights the primary features of the CL PX2070 when operating in each of the three bus in

NOTE: Field HSB of Register HtU_CSU specifies which of the three weerlaces is to be used Table 3-2. CL-PX2070 System Interface Highlights

	ISA Bus Interface	MCA Bus Interface	Local Hardware Interface
Interface	CL. PX2070 interfaces with the host system interface bus as shown in Figure 3.7	osi sysiem interface bus as	CL PX2070 resides on the lucul
Multiplex Support	Address and data buses are multiplexed. CL. PX2010 provides Seprats DDHR and DEN" to support the required host system address/data multiplexing, and to provide bothrectional buffering the host system data bus as shown in Figure 3.1	Address and data buses are mutiplesed CL PX20/0 provides Sograss DDHs and DE N° to support the required host system address/data mutiplesing, and to provide biolercitonal buflering of the host system data bus as shown in Figure 3-7.	The data bu
Address	CL PX2010 internally decodes the bus address during system cycles. Table 3-4 lists the primary and secondary I/O address maps, selected during configuration, and the HIU Hegisters mapped to each	Ct. PX2010 enternally decodes the bus address during system I/O cycles. Table 3-4 hats the primary and secondary I/O address maps, selected during configuration, and the HIU Hegisters mapped to each.	The host processor provides in the thost processor provides CS to enable the CL 14/20/0 nost enable th
Register	Cr.Px20	CL. PX2070 supports standard register access cycles	SS Cycles
DMA	DMA through direct memory port	No DMA support DMA through port	DMA through indexed memory port

80 160 £ 1003 1458 05 03 ā ē CL P1/2070 PE SE I

HE SE

Figure 3-3. External Configuration

Default (Local) Configuration

The CL PX2070 selects default (local) contiguration when FBD(5:3) are high. This configuration, shown in Figure 5.4, causes the host system bus to default to local hardware interface mode. A fixed, default configuration of all bits high is loaded into the LSB of Register HIU_CSU, automatically providing the default configuration dataset. FBD(5:0) are internally pulled up.

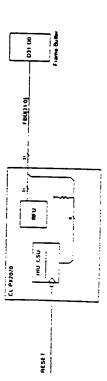


Figure 3-4. Default (Local) Configuration

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CL-PX2070 The bus interface signals share a common set of VO pins, as shown in Table 3-3. For a complete pin assignment table, refer to Section 1.2 on page 15. Video Provessor

Table 3-3. Host System Bus I/O Pins

32 AEN I MYO' 33 MCS'* I CARDEN 35 ROH" I SI' 36 ROW" I SO' 37 DMACK' I CUSE UBB 39 ROIG' O CUSE UBB 39 ROIG' O CUSE UBB 40 LINDY O COCHID 41 RESET I CONUSE 43 DDIR O UDBR	_					
	YEN.	-	.Oum	_	.sɔ	•
0 0 0 0	ğ		ADL:	-	ASIZI	•
0 0 0 0	AUXCS	-	CANDEN	-	Icisu	_
0000		-	31.	_	OR.	-
0000	ě.	-	.3	-	.MOH	-
0 0 0	DMACK	-	COSETUP.	-	DMACK.	-
0 0	CHARGO	0	COSF DOK	0	DMARO.	0
0 0	.910	0	.91 SOOO	0	S.	ŀ
0	CHRUY	0	COCHIDA	0	CHRDY.	0
- 0	BCIK		CMD.	_	PCLK	-
0	HESE	-	CORE SE 1	_	RESE T	•
	PIOC	0	HIGO	0	BLAST.	-
44 DEN O DEN	DEN	0	SEN.	0	เปรเป	•
45 190 0 1910.	Q.	0	EKO.	0	Но.	0
48 62, 65 SADI 15 01 VO AU[15 0]	SADIS		AU[15 0]	Q.	0 5 0	Ç,

a AUXCS* is used in AUX ISA mode. SA(I)[3.0] are used to address individual registers

Video Processor CL.PX2070

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ISA Bus Interface

The CL-PX2070 interfaces with an ISA Bus using the pins tisted in the Pin Assignment Table on paye 15. The CL-PX2070 insponds to VO mapped bus cycles, including register access cycles and DMA cycles. Register access cycles. The CL-PX2070 multiplexes the system address (SAL5 0) and data (SU[15 u)) buses to Bus SAD[15 0] using external butters controlled by Signals DDH and DEN. Figure 3.5 shows the signal relationship for the ISA Bus mediace for register access cycles.

NOTE: BALE is shown only for reference — it is not used, At N + U WRITE DATA SACTISOS ě. Š

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Figure 3-5. ISA Bus Interface for Register Access Cycles

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UMA cycles. The CL. PX2070 supports high spend DMA cycles for bidiscribinal data transfer between the host system and the Frame Builter. The Cl. PX2070 must be programmed for DMA mode using Register. HIU. DCS. Figure 3 6 shows the signals and general timing for the ISA Bus interface for DMA cycles.

DAMACK. ¥ COM . C

Video Provessor CL-PX2070

C1.-PX2070 Video Processor



The lower eight bits of the CL PX20/0 address bus is multiplexed with the data bus Fujure 3.1 shows a method of interfacing the CL-PX20/0 with the separate address and data buses of ISA. A similar circuit can be used to interface to the MCA Bus.

S ISA Bus

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Figure 3-7. ISA and MCA Interface Address/Data Multiplexers

Figure 3-6. ISA Bus Interface for DMA Cycles

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CL-PX2070 Video Processor



Video Processor CL-PX2070

The CL-PX2070 intoffaces with a local processor using the pins shown in the Pin Assignment Table on page 16, The CL-PX2070 responds as an IVO device to register access cycles and DMA cycles. or may be used as a memory mapped device. Figure 3 shows the general inning for a register write, and Figure 3 to shows the timing for a read cycle. Local Hardware Interface

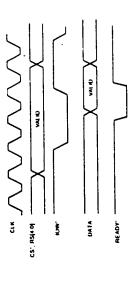


Figure 3-9. Local Hardware Interface Write Cycle

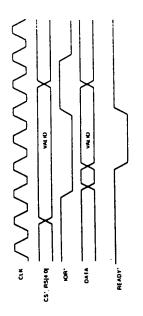
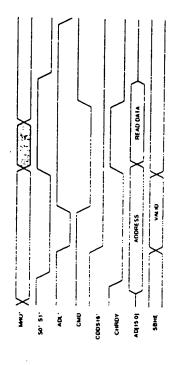


Figure 3-10, Read Timing (Local Hardware Interface)

MCA Bus Interface

The CL PX2070 interfaces with an MCA Bus using the pins shown in the Pin Assignment Table on page 15. The CL PX2070 responds only to I/O-mapped bus cycles. Register access cycles. The Ct. PX2070 multiplenes the system address (A115.0I) and data (D[15.0I) buses to Bus AD[15.0I using external buffers controlled by Signals DDIR and DER* Figure 3.8 shows the general timing for register access cycles. Refer to the detailed signal description on page 19 for the MCA Bus cycle decoding performed for Signals M/O., S0*, and S1*.



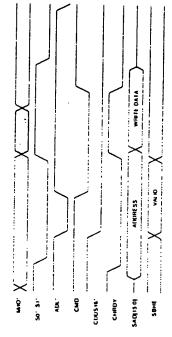


Figure 3.9. MCA Bus Interface for Register Access Cycles

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DMA cycles. The CL PX2070 supports high speed DMA cycles for butherchorial data transfer between the host system and the Frame Buffer. The CL:-PX2070 must be programmed for DMA mode using Register HIU, OCS. Figure 3.11 shows the signals and general liming for DMA cycles.

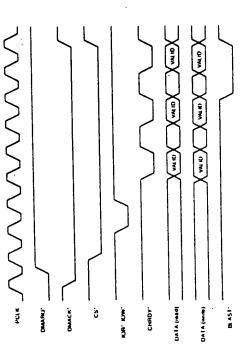


Figure 3-11, Local Hardware Interface DMA Cycles

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3.1.1.3 Frame Buffer Configuration

No operational changes are required on the part of the CL PX20/0 between a design using a DHAM frame builder and one using VRAM. The use of VRAM in a system based on the CL PX20/0 and the CL PX2080 enables the full range of features. Field FBT of Register HIU. CSU is provided so that the timinware can determine the hardware configuration in which it is operating and adjust the available features. accordingly. FBT defaults to VRAM.

3.1.1.4 Port Address Configuration

Table 3-4 shows the port address configurations for ISA, MCA, and Local Hardware interlace Modes. As shown in Table 3-1 on Page 27, field PAS of Register Httl/ CSU specifies whether the host system uses the primary or secondary I/O address map when accessing the CL PX20/0 in ISA or MCA Modes (PAS). is not active in Local Hardware Interface Mode).

Table 3-4. VO Address Maps

	ISA and MCA Interfaces	MCA 13	Local H/W Interface		
Register Pri	Ē	280	RS(3:1)	Used By Registers	jisters
0. DIE	27C9n	27C0n 0290n	8	HRU CSU HRU DBG HIU DRD	Configuration Solup (Road Only) Debug Control (Write (Inly) Debug Read (Read Only)
- OH	27C2h	42620	£	HIU OCS	Operation Control/Status (Read Write Interrupt Status (Read Only)
180.2	27C4h 0294h	2/C4h 0294h	₹.	NE DIN	Register Index (Nead-Write)
1#U.3	27C6h	0296h	£	HIU RD1	Register (Jata Port (RenduWrite)
HIU.	27CBh	0296h	\$	HU MDF	Memory Data (Read/Write)

3.1.2 Register and Frame Buffer Interface

Regardless of whether the CL. PX2070 is operating in ISA, MCA, or focal hardware interface thote; the CPU regards it as the five 16-bit registers defined in Table 3.4. These registers allow access to all CL.PX2070 data registers and to the Frame Buffer.

- HIU_0 and HIU_1 control configuration and setup, overall operation, general status, Jint interrupt sta
- · HILL 2 and HILL, 3 allow the host system to access the data registers
- HIU_2 is the index, which points to the internal register to be accessed in the next I/O cycle.
- HIU_3 is the data port.
- HIU 4 is a frame buffer memory data port.

3.1.2.1 Internal Register Access

To read an internal register, the CPU writes the index address of the dissinct register specified by HitL. 2. U. RIN). If their leads HILL 3 (HILL RDT), returning the value sfored in the register specified by HILL. 2. When autoincrement is enabled in HILL 3, the index value in HILL. 2 increments after each access, altining. ing a group of configuous registers to be loaded with a block transfer

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3.1.2.2 Accessing the Frame Buffer

bansker, providing a pointer to a specific location in memory. A subsequent access to HIU, 4 reads from or writes to the address associated with that buffer, taking advantage of the direct access that the HIU. to access the frame buffer, the CPU sets up an object buffer in the Reference Frame Unit for a block has to an input and an output FIFO within the VPU.

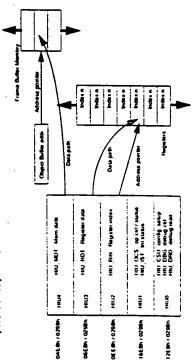


Figure 3-12. Register Access

For additional information on the Index and Data Registers, see also.

- Table 4.3 HIU Registers Accessed by the Register Data Port, p. 81
- Table 4 4 VBU Registers Accessed by the Register Data Port, p 90
- Table 4-5 VPU Registers Accessed by the Register Data Port, p. 100
 - Table 4 6. RFU registers Accessed by the Register Data Port, p. 136

 - HIU RIN Register Index (Read/Write), page 87
 - HIU_ROT. Register Data Port, page 88.

3.2 VBU: Video Bus Unit

The VBU, shown in Figure 3-1, manages the flow of video and graphic streams between the CL PX2070 and up to three independent devices (including the host system). It also provides a data path between the CL-PX2070 and the host system for bidirectional graphic streams through the HIU.

lailed in the following sections:

The VBU prowdes two independent, real-time video I/O ports and contains two subunits, which are de-

- VIU: Video Interface Unit. The VIU controls the flow of video data streams between the VPU and exernal video devices.
- VSU. Video Sync Unit. The VSU has independent sync signals for both video ports. Signal polarity

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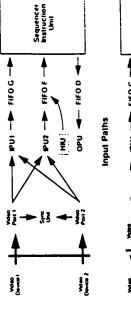
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and direction are programmable.

In addition, three functional blocks within the Video Processing Unit (VPU) are closely related to the func-tionality of the VBU because of their 40 involvement. Each of these blocks and their associated fit ()s can be connected to either V1 or V2 under sollware control. For additional information concerning the VPU and its functional units, refer to Section 3.3 on page 46.

- Input Processing Unit I (IPU1) performs scaling, format conversion, window chipping, and color spure conversion. FIFO G is IPU1's output. It leeds a data stream to the Sequencer Instruction Unit it the VPU. See Section 3.3.2 on page 50 for additional information.
 - Input Processing Unit 2 (IPU2) performs window clapping only. FIFO Fis IPU2's output. It feeds a thits stream to the Sequencer Instruction Unit (SRJ), also located in the VPU. See Section 3.3.3 on puyer
- into IPU1 or IPU2. The OPU can act as sync stave, with outputs conforming to incoming video, if pre The Output Processor Unit (OPU) receives data through FIFO D. The OPU can be connected back ferred. See Section 3.3.5 on page 68 for additional information 60 for additional information.

Figure 3.13 illustrates the possable input and output paths (shown separately for simplicity) for video duta in addition to these paths. FIFO D can send to and FIFO F can receive from the HIU directly



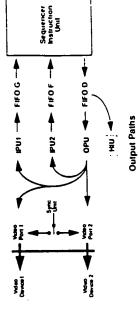


Figure 3-13, Possible Paths for Video Data

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3.2.1 Videa Ports V1 and V2

The VBU provides two 16 bit digital video ports — V1 and V2. Either port can be used with the VSU at any single point in time. V1 and V2 have the following characteristics:

- can be configured as input only, output only, or pixel: or field-duplexed I/O;
 - provide programmable sync polanity;
- either port at one time can use the sync generator provided by the CL PX2070;
- 16 bit YCbCr, 12 bit YCbCr, 16 bit RGB, 8 bit RGB (input), support the following formats:
 - 16-bit YCbCr, 16 bit RGB, 8 bit RGB (output);
- V2 controls the video stream data flow between the CL-PX2070 and typical CODEC devices using Signals STALL" and STALLHO".

3.2.2 VIU: Video Interface Unit

The VIU controls the flow of video data streams between the VPU and external video devices. It specifies:

- The source and direction of video stream and sync control inputs.
 - the field toggling mode and field ID signals,
 - · the watchdog timer feature.

3.2.2.1 Video Stream and Sync Control Inputs

As shown in Figure 3.1, the VIU contrats the flow of video streams through video ports V1 and V2 to all external devices, as well as the flow of internal streams. An input multipleare directs one of two input streams of the output stream of the OPU to the input of the IT-U1. A second input multipleare directs one of two input streams or the output stream of the OPU to the input of the IP-U2. A pair of buffers can output a stream from the output of the OPU to V1 or V2.

These functions are performed by the registers specified in Table 3.5

trom FIFO D to the HIU, bypassing the OPU

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Table 3-5. Video Stream and Sync Control Inputs — Control Registers

Register	Field	Function
VIU_MCRp	MQ.	Impus/Output Mode Specifies the direction of video stream data flow through wideo ports VI and VZ. Each port can be programmed as input only, output orth; or as dispersed for under me control of Signal Vigit II. MOTE: Each wideo poor provides input enable Signal Vigit IV. It is control the grammed as topy provides input enable Signal Vigit IV. It is control the population of grammed as tour long. You specified and long in the port is programmed as output only. Vigit IV is desistented and lead with IT is possible to modes are also provided Depending on the control policity in specified for president prose in pass model Signal Vigit IV is driven to entire in altin or be a compensation or input Signal Vigit IV is driven to entire in altin or be a complement of input Signal Vigit IV is driven to entire in altin or be a complement of input Signal Vigit IV.
VIU_DPCI	PUIDC	PUT Databath Cortol Specifies the video stream and sync control riplas of the PUT PUT stream data and control sync can be driven by either VI or V2. The reput stream optionally can be qualified by Signal PVPT When the QPUT is specified as the source of the input stream, the sync references are provided by the internal sync generator. See also VSU Video Sync Unit, puge 43.
VIU_DPC!	PU2DC	PUZ Datapath Control Specifies the stream and sync control rights of the INVD IPUZ stream data and control sync can be driven by either V to V V The what stream data and control sync can be driven by either V to V V The what stream optionable you be qualified by Sopial VLPH I he stream data stiss can be driven from the OPU stypial VLPH I he stream data stiss can be driven from the OPU is specified as the source of the what stream the sync celements are provided by the internal sync generator See also VSU Video Sync Unit page 43.
VIU_DPC!	200	ODC Databath Control Specifies the control sync source for the struam output from the OPU. A stream can also output to the host system by flowing directly

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3.2.2.2 Field Toggling and Field ID

The VPU subunits IPU1, IPU2, ALU, and OPU each contain parallel sets of registers (i.e., ALU Master Control Registers ALU MCR1 and ALU MCR2), altowing the CL-PX20/0 to perform different operations on two independent, single-field video streams during a common frame time.

The StU is the only VPU subunit that does not contain dual processors, but it does have a field toggle feature that distinguishes between the vertical sync pulses for each field and executes one of two different instruction sequences. This dual held toggle feature requires a signat that specifies the set or field to be

The held synchronization signal is the master sync signal for the VPU; it is used to derive two signats:

- Field ID Signal FID. The state of this internal signal (in intertaced mode) is determined by the sync signals, in non-interdaced mode this value remains at 0. FID apecifies the register set that its to be used in the IPU2. ALU, and OPU; it is shown in Figure 3-16, Figure 3-17, and Figure 3-24.
- Field Topple Signal. This signal determines whether the StU selects field 1 or field 2. See also: StU: Sequencer Instruction Unit, page 46.

These functions are performed by the register specified in Table 3.6.

Table 3.6. Field Toggling and Field ID — Control Registers

Register	Fletd	Function
VIU WDI	MFTS	Master Field Toggle Select. Speciles whether the VPU is to determine its held synchronization signal from the vertical sync puise on: video port V1. video port V2. video port V2. video port V3. video port V3. video port V6. video port V6. video port V6. video port V7. video port V7. video port V8. video p
		streams without sync controls). software command. See Section 4.2 1.3 on page 94.

3.2.2.3 Watchdog Timer

can emutate sync references for streams which have no sync (such as graphic stream data to or from the The VRU's watchdog transfer can generate a watchdog trans signal to detect a loss-of-sync condition, or it

its functions are performed by the register lields specified in Table 3.7.

Table 3-7. Watchdog Timer — Control Registers

Register	Field	Function
VILJ. WDT	WIE	Watchdog Timer Enable. Enables or disables the operation of the watchdog timer. Disabling and then re enabling results the counter to the programmed value.
VIU. WOT	1MOU!	VIU. WOT TMOUT Timeout interval. Specifies the 10 bit lemeout period count of the watchdoog timer. This count is based on the input memory clock Signal MCLK MCLK is prescaled by a factor of 49, ISS (3 * 214) for use by the inneout counter. Assuming a 80 Mill water for Signal MCLK, the bineout range a valiable would be from 0.62 ms. TMOUT count = 110 838 ms (TMOUT count = 1023).

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3.2.3 VSU: Video Sync Unil

The Video Sync Unit (VSU) has independent sync signals for both video ports. Signal polarity and direc tion are programmable.

The VSU implements identical, independent video reference signals for each video port

- VpVS (vertical composite sync) -- bidirectional video sync signal that identities the beginning of a link) (intertaced stream) or frame (non-intertaced stream);
 - VpHS (norizontal sync) bidirectional video sync signal that identifies the beginning of a line,
- VpHB (horizontatcomposite blanking) input or output signal that specifies the horizontaticomposite blanking interval.

Each video port implements independent control of sync potarity for each of these signals. Master cuntrol Registers VIU_MCRp provide matching fields that specify input and output sync modes, as shown in Ta

Table 3-8. Input and Output Sync Modes — Control Registers

Registers	Fleids	Function
Output Sync Modes	Kodes	
VIU_MCRp	OVSP	Output Video Vertical Sync Polarity. Specifies potanty of vertical sync signals VIVS (VIU, MCR1) and V2VS (VII), MCR2) when socials are used as output
VIU_MCRp	OHSP	
VIU_MCRp	980	Output Video Blank Polerity. Specifies polarity of horizontalicumposite blank ing Signats VIBL (VIU, MCR1) and V2BL (VIU, MCR2) when signals are used as output
VIU_MCRp	180	Output Video Blank Type. Specifies horizonlai/composie bainking signals VIBL (VIL) MCR1) and VZBL (VIU MCR2) to be either i libank or Cluank when signals are used as output
Input Sync Modes	lodee	
VIU_MCRp	NSP	broad Vertical Sync Potarity. Specifies potarity of vertical sync Signals VIVS (VII) MCR1) and V2VS (VII) MCR2) when suprais are used as intuit
VIU_MCRp	HSP	Input Video Horizontal Sync Polarity. Species pularity of horizontal sync Signate VIHS (VII), MCR1) and V2HS (VII), MCR1) when signals are used as input.
VIU_MCRp	d.	Input Video Blank Polanity: Spechos polany of honzonlatromposie Eusiminy Sgnass v IBL (vru.) MCR1) and v28L (vru.) MCR3) when signals are used as input
VIU_MCRp	19	v, =

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The VSU implements an internal sync generator to provide the horizontal and vertical references, listed in Table 3-9, when the CL PX2070 is programmed as a sync master (see Figure 3-14). The references can then be discorded to VL VZ, if VL1 or IPVZ. Flets the UDLOC and IPUZOC in Register VIU. DPCI specify the horizontal binetase reference to the internal sync generator as either MCLK/G or as MCLK/6 when the OPV sources the data stream to IPV1 or IPV2. The OPV must always be programmed with the VSU internal syncs if it outputs to the IPV1 or IPV2 data paths.

Table 3-9. Horizontal and Vertical References — Control Registers

Register		
	Fletd	Function
Horizontal References	rences	
- dii nsa		Horizontal Period. Species the lotal number of horizontal timebase clock periods in the horizontal interval. WOTE: The actual period is the number entered in this held plus one
- WSII ÎNSA		Horizontal Sync Width. Species the number of horizontal timebase clock part- ods for the interval of the horizontal sync pulse.
VSU_HAD		Horizontal Active Delay. Specifies the number of horizontal timebase clock pelinds for the interval between the beginning of the horizontal sync pulse and the beginning of active pure period.
HIAP		Horizontal Active Plade. Species the number of horizontal timebase clock periods for the interval of active pirets per line.
Vertical References		
- da nsa		Ventical Period. Specifies the lotal number of horizontal sync intervals in the ventical interval.
vsu_vsw		Verifical Sync Width. Specifies the number of horizonal sync intervals for the interval of the vertical sync pulse
VSU_VAD		Vertical Active Delay. Specifies the number of houronial sync intervals for the interval between the beginning of the venical sync pulse and the beginning of active time period.

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VSU HAP VSU INP.1 VSU HAD VSU. HSW

VSU VAP VSU VP VSU_VAD WSW USW Versial Sync NOTE: In this example, the VIU_MCR sync polarity bits are programmed us 1, for untivit light syrin.

Figure 3-14, Programmability of the Internal Sync Generator

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Vertical Active Pixels. Specifies the number of horizontal sync intervals for the interval of active lows per held (interfaced) or frame (non-interfaced)



3.3 VPU: Video Processor Unit

up to two external, bidirectional real time video streams and a single external, bidirectional host video or The VPU, shown in Figure 3-1, provides held oriented video processing. It can simultaneously process.

The VPU contains the Master Control Register VPU, MCR (described in section 4.3.1, page 105), and live Subunits, each of which is detailed in the following subsections:

- SIU: Sequencer Instruction Unit
 - PU1: Input Processor Unit 1
 - IPU2: Input Processor Unit 2
- ALU: Arithmetic and Logic Urut OPU: Output Processor Unit.

IPU1, IPU2, and the OPU provide the video data paths between video ports V1 and V2 and the SIU. The SIU moves data between the hardware resources. The ALU can operate on purets logically or arithmell-cally, replace a pixel or one of its component values with a constant, and decode and/or encode pixels

3.3.1 SIU: Sequencer Instruction Unit

The Situ is a special purpose microconitoller that moves pixel data between the hardware resources under the control of instruction sequences stored in the SIM.

The SIU resembles a short soliware loop made of conditional instructions. Each instruction causes data to move between the components listed in Table 3.10, and specifies.

- the source of the video information,
 - conditions for execution, destination, and
 - the location of the next instruction.

Possible sources and destinations are object bullers and FIFOs A ${f G}_{\rm c}$

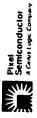
Table 3-10. CL-PX2070 FIFOs

Dedicated FIFO Component

FIFO Depth		so chies	126 bytes	64 byles	120 bytes	NA	
Dedicated FIFO	FIFOG	FIFOF		THOS A. B. C. E	1000	XX	
	IPUT Input Processor Unit 1	PUZ Irput Processor Unit 2	ALU Anthroebe and Logic Unit	OPU Output Processor Line	OBU Object Buffer Uni		

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FIFO essociation: Specifies Figure 3-15 is an overview of SIU instruction flow.

which fift House that fift Os-automatic uly read from OBU, output fill Os with to OBU

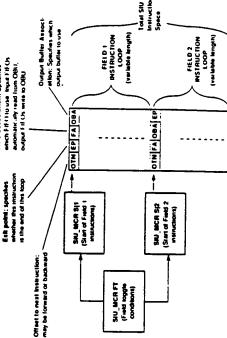


Figure 3-15. StU Instruction Flow

or may not be ready to source or receive data. If it is not ready, the SitU stups the instruction and continues with the next until an instruction is found which can be executed. The SIU can execute SIM instructions much faster than the sugarn rates of typical video data. Therefore, the instructions are conditional. At any given time, the FiFO associated with the current instruction may

internal OBU controls allow a stream being written from an output FIFO to an object builter to be semula neously copied to an input FIFO, reducing data path trailic in recursive processing operations

The following sections detail the major components and functions of the SIU.

- Programming the SIU
- Master Control Register StU_MCR
- Sequencer Instruction Memory SIUs_SIM
 - Accessing FIFO Control/Status Indicators.
- 3.3.1.1 Programming the SIU

- The SIU can be programmed for all the following operations a single instruction sequence loop used to process
 - a single non-interlaced stream, or
- one or both fields of an interlaced stream.

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two instruction sequence loops used to process ...

- two different, non-interlaced streams.
- a single non-interfaced stream and a single field from an interfaced stream,
 - -- both lields of a single interlaced stream, or

 - a single field each from two different, interlaced streams; multiple instruction sequences used to process...
 - an arbitrary number of streams.

To program the SRU, determine the path of the video stream and plan the desired conversions. Then all focate the various hardware resources and configure them accordingly.

The SIU can be programmed to be field time controlled. That is, it can execute one sequence loop in the even field time, and another sequence loop in the odd field time. (See also: Field Toggling and Field tiD. page 42)

Because the StU is feld based, the controlling software application must specify the source of the vertical sync pulse that performs the field loggle, and whether other steam processing is to be performed at the same time Field MFTS of Register VIU_WDT specifies the source of the sync signal used for the field loggle, as shown in Table 3.6.

3.3.1.2 Master Control Register StU_MCR

Master Control Register SIU. MCR directs entry points into the SIU for sequencer cycling. It performs the functions specified in Table 3-11.

Table 3-11. Master Control Register SIU_MCR

Register	Field	Function
SIU_MCR	IIS	Start Index 1. Specifies a start instruction index for Field Time 1. The value in SI1 is the index in the SIA of the first instruction executed in Field Time 1.
SIU_MCR	215	Slart Index 2. Specifies a start instruction index for field Irine 2. The value in SI2 is the index in the SIM of the first instruction executed in Field Time 2.
SIU_MCR	14	Field Toggle. Specials four modes of held timing sync. No held toggle (S1 is used. SI2 a ignored). S1 and SI2 toggle on ventral sync. no field association. Field 1 is associated to S1, and helds 1 and 2 toggle on ventral sync. Field 2 is associated to S1, and helds 1 and 2 toggle on ventral sync.
SIU. INCR	SE	Sequencer Enable, Haits the SIU, or specifies that the SIU start on held SII or

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3.3.1.3 Sequencer Instruction Memory SIUs_SIM

Sequencer instruction Memory SIUs, SIM is a register file that stores the sequence instruction. It contains 32 identical 16-bit registers, indexed from 0 to 31 (SIM[31 0]). Each register stores one instruction that contains four fields, as described in Table 3-12.

Table 3-12. SIUs_SIM Instruction Fields

Function

Field

Register

SIUS_SIM	NTO	Ottaet to Next Instruction. Specifies the signed, 5 bit officet to the next instruc- bon. This value can be positive or negative (to implement a simple loop), and is added to the current instruction index to operate the mote of the next instruc- tion is execute. For example, if Shiff(s) is the current instruction and has an OTN value of -3. Shiff(s) will be the next instruction executed.
SIUs_SIM	a	Exit Point. Species that the current instruction is the exit point of the current sequence toop.
SIUS_SIM	¥.	FIFO Association. Specifies the source or destination fill Office to current instruction. Secondary 8 for on order buffer, this implying a detaction for example, associating an output left to an object buffer, mighted a write operation from the FIFO to the object buffer.
SrUs_SIM	V80	Object Buffer Association. Specifies the corresponding destination or source object buffer for the current instruction.

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3.3.1.4 Accessing FIFO Control Status Indicators

Each FIFO has lour flags which the controlling software application can access through the two SIU Reg. isters described in Table 3-13

Table 3-13. Accessing FiFO Control/Status Indicators — Control Registers

FIFO Control/Status, Returns the current tull and empty status flags. Writing to any of the FIFO empty hatds (FIE) hatts and resets the corresponding FIFO. See also, SNL_FCS, FIFO Control/Status, page 124. FIFO Overflow/Underflow. Provides access to the overflow and underflow Function Field Register SRU, FOU

Register StU, FCS is a special read/write register. On read, the status hags are returned. During a write, only the FLE helds are used to reset the FIFO. The reset values cannot be read bach, so the controlling soft-ware application must retain a copy.

3.3.2 IPU1: Input Processor Unit 1

The IPU1, shown in Figure 3.16, prepares an input video stream for ALU processing and/or storage in the Frame Butler, then outputs the prepared stream through FIFO G to the Frame Butler Data Bus. Its video processing features include YCbCr and RGB input stream format conversion, color space conversion, programmable data lagging, three channel tookup table operations, horizontal prescaling, window dipporting, horizontal and vertical scaling, and output stream format conversion.

The IPU1 has two Masier Control Registers (IPU1 MCR1 and IPU1 MCR2), allowing the IPU1 to perform different operations on two independent, single-held video streams during a common frame time. Field ID Signal FID, shown in Figure 3, 16, determines the register set to be used. See also: Field Togging and Field ID, page 42.

The IPU1 contains seven subunits, each of which is detailed in the following paragraphs:

- 6input Formal Converter and Chrominance Interpolator

 - Input Tag Unit
- Color Space Converter
- LUT RAM
- Window Chipping and XY Scaler

X Prescaler

Output Format Converter Unit.

This section also describes the IPU1 Interrupt Request Unit.

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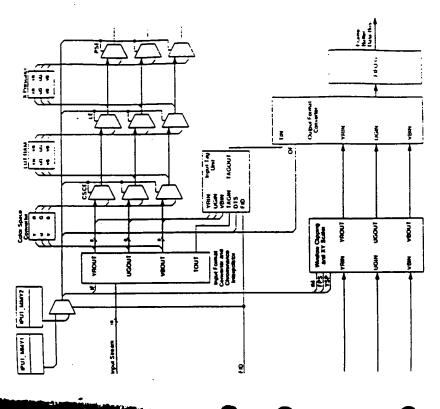


Figure 3-16. IPU1: Input Processor Unit 1

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3.3.2.1 Input Format Converter and Chrominance Interpolator

The Input Format Converter and Chrominance Interpolator, shown in Figure 3-16, has two functions:

The Imput Format Convertor operates on external and internal streams. It produces three 8-bit and one 1-bit lag buses that are used exclusively by the other IPU1 subunits. These lag buses do not appear outside the IPU1:

. The Chrominance Interpolator

Input Formal Converter

The Imput Format Converter demultiplexes 16 bit 4:2:2 or 12-bit 4:1:1 YCbCr video data into the non-mulspleased formal used by IPU1 (8-bit YR, UG, and VB buses with a 1-bit lag, as shown in Figure 3-16). The Input Formal Converter accepts as input:

the YCbCr video input stream formats defined in Table 3-14.

the 16 bit RGB video input stream formals defined in Table 3-15, and

the pseudocolor video input stream format defined in Table 3-16.

These formats are specified by field IF in Registers IPU1_MCRI for each field time.

MOTE: These specified input formats do not imply that the Input Format Converter performs color space conversion A specified VCBCs format implies that the stream input for processing with the ni VCBCs format. A specified HGB format implies that the stream input for processing will be in RGB format. The controlling software application must ensure that the desired processing its compatible with input video stream.

Table 3-14. YCbCr Video Input Stream Formats

The Video input Subam Formats in this table are shown for four consecutive VpCLK clocks $C_{\Gamma}\cdot C_{\phi}$

4:1:1 YCbCr Non-Tegged VpD CLK, CLK, CLK, CLK, CLK, CIK, CLK, 4:2:2 YCbCr Tagged 4 2:2 YCBC/ Non-Tagged CLM, CLM, VPD

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Table 3-13. 10-01 Note when when the court of the														
9:6:5 RGI VpO	Mon-Ta	gr.	CLK,	CLK,	9:5:5 RGB Vp0	Non-Tagger CLX, CL	CLK,		כוא, כוא,	5.5 5 ROB Tagged VpO CLK,	Tagged CLK,	CLK,	כוג, כוג	Ç,
200	à	á	'n	à	\$100	۱,	:	,		VpD15	۔	-	-	٠.
4	8	é	É	8	VPD14	Я,	₽,	Н,	ì	VpD14	ŧ	£,	ě	₹
1000	ź	ž	. £		VeD13	9	18	, E	£	VpD13	He,	18	9	ž.
200	ž	ź	ž	ž	Vp012	£	ŝ,	H3,	£	VpD12	£,	H2,	£,	Ė
Cox	2	5	Ę	5	Vp011	ž	ž	ź	÷	Vp011	Ě	ž	į	į
01007	9	ò	6	6	VpD10	3	£,	Ę	Н3,	VpD10	E.	нэ,	£	Ē
o Guy	ð	ð	ð	3	VpD9	ô	Ġ	6	6	Vp09	ò	3	3	3
VaDa	8	S	9	ŝ	Noo.	ś	3	ģ	3	Np08	Š	Š	ś	:
Vooy	ð	3	ð	้อ	Voov	ŝ	69	6	S _S	Vooy	S	ŝ	ŝ	ទ
Vo0	8	3	S	ទ	Vp06	8	ŏ	ð	ċ	VpD6	ö	3	į	ĕ
5002	6	3	ö	25	V 005	ŝ	ŝ	ś	ç	VpOs	3	Ğ	ŝ	3
Vo V	8	6		6,7	900	6	ě,	6	6,	VpD4	æ	6 /8	é	æ
500	Z	á	ž		VpO3	96	8	8	8	COdy	8	H6,	ě	ż
VoD2	8	98	8	95,	Vp02	95,	63,	9	95	Vp02	68	e,	63,	ŝ
VoO.	ā	ž	ž	8	100	4	ě	ě,	4	VpD1	ă	θ,	ž	ě
V _o D _o V	6	2	, E	93,	VPD0	93	69	6	6	00dy	6	e,	é	â

Table 3-16. 8-bit Pseudocolor Video Input Stream Formats

Shir Pseudocolor Non-Tegged (Muliplaned a,b) VpD C₍₄₃

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The Chrommance Interpolator accepts the following input data formats. Chrominance Interpolator

- rate of the Cb and Cr channels with a low pass fitter function to produce the equivalent of a 4:4.4 YCb. 4.2.2 YCbCr When 4.2.2 YCt.Cr data is input, the Chromhance Interpolator increases the sample
- stream, then outputs it to the chrominance littler for processing (this process is automatic when 4:1:1 YCBCr data is specified). All results are rounded to 8 bits. Values less than 0 are set to 0, and values 4.1.1 YCbCr. The Chrominance Interpolator lirst converts 4:1:1 YCbCr data into a 4:2:2 YCbCr greater than 255 are set to 255.
 - Ø ber pseudocober, When the 8 bit pseudocolor input data format is specified, the input Format Converter replicates the input 8 bit piret value to all three 8-bit channels (primarity for the use of the Color Space Converter in producing 24 bit RGB or YCbCr data).

3.3.2.2 Imput Tag Unit

The knpul Tag Unit, shown in Figure 3-17, implements independent YCbCr chroma key tagging on the input data stream. A complete register set (IPU1_MCR1 through IPU1_MMV1, IPU1_MCR2 through IP-U1_MMV2, as shown in Table 4-6) is provided for each field time to independently tag fields 1 and 2.

Field ODT in Registers IPU1_MCRt specifies four tagging modes:

- existing input stream (if any) remains unchanged.
- imput stream is tagged with the ID of the current field (0 = field 1, 1 = field 2).
 - exput stream is tagged with the output of the chroma key multiplexer.
- input stream is tagged with the inverse of the chroma key multiplexer.

discriminate pixel values found between the programmable 8 bit minimum and maximum values defined three independent, identical chroma key comparator circuits -- one for each of three input channels -in Registers IPU1, MMY1, IPU1, MMI11, and IPU1, MMV1. As shown in Figure 3-17, the output of each comparator circuit selects one of the four inputs to the chroma key multiplexer.

The inputs of the comparator circuits are also programmable using Registers IPU1_KFC1. This flexibility alows the input stream to be lagged according to a pixel data value for any of the bries channels inde-pendently, or for any independent combination of pixel values found on the three channels.

Color Space Converter

of 128 identifies the 0 point within a range of 225 quantization levels for the Cr and Cb channels. The result is rounded to 8 bits -- values less than 0 are set to 0, and values greater than 255 are set to 255. Fields The Cotor Space Converter transforms YCbCr prixel values into the equivalent RGB prixel values using the iers of Digital Television" Excess 128 notation is assumed to be used for the Cr and Cb channels. The value functions specified in The International Telecommunications Union Recommendation 601-1. Encoding Parame-CSCE in Registers IPU1 MCHI specify whether the Color Space Converter is enabled or bypassed for each held time.

3.3.2.4 LUT RAM

The LUT RAM is a programmable Look Up Table (LUT) comprised of three independent, 8-bit channels, each containing 256 8 bit read/write elements. Each LUT accepts input from one of the 8-bit output chan. nels of the Input Formal Conventer

The LUT HAM performs the following functions.

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- Fields LE in Registers IPU1_MCRI specify whether the LUT RAM is enabled or bypassed for each held point transforming (any input to output pixel mapping dependent on the input pixel value)
- Athough the LUT FAM can be enabled on bypassed indepentiently each held time, only one loukup furth ton is possible during both helds times. Therefore, the controlling software application must either priform denical operations during both held times, or bypass the LUT HAM during one held time. MOTE

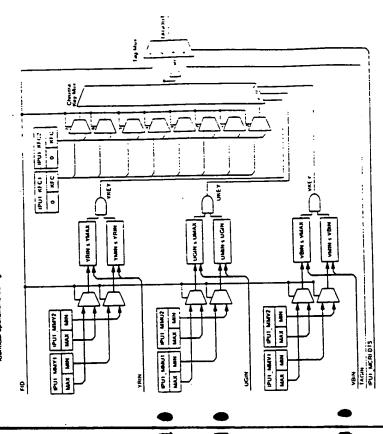


Figure 3-17. Input Tag Unit

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3.3.2.5 X Prescaler

mains unchanged. Fields PSE within Registers IPU1_MCRI specify whether the X Prescaler is enabled the X Prescater is a 2:1 decimator; that is, it drops all even numbered pixels. Data along the Y axis reor bypassed.

3.3.2.6 Window Clipping and XY Scaler

The Window Clipping and XY Scaler, shown in Figure 3-18, has two functions:

- The IPU1 Window Clipping Unit clips the Input stream into a rectangular region.
- -- The Y Scaler uses a nearest neighbor (decimation) algorithm to selectively drop full rows from the input stream (A Special Y Scaling Path Mode using interpolation is described on page 57.) The Y Scaler and X Scaler perform independent vertical and horizontal scaling.
 - The X Scaler uses tinear interpotation for horizontal scaling.

Registers within the Window Chipping and XY Scaler define the chipping window coordinates and the X and Y scaling values for each field time.

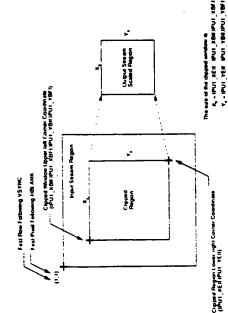


Figure 3-18, Window Clipping and XY Scaling Control Registers

H, - HC/1PUI_SCRIPUI_HSFI V, - Yc/1PUI_SCRIPUI_YSFI

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PU1 Window Clipping Unit

The Window Cipping Unit defines the cipping window — a rectargular area in the rigur wideo taria stream. The cipping window can be a region of only a few pixels per side, up to the entire inquit stream. and is defined by the following registers:

- Registers IPU1_XBnf and IPU1_YBnf specify the upper left corner of the choping window
- Registers IPU1_XEII and IPU1_YEII specify the fower right corner of the chipping window
- X and Y scaling logic processes only those pixels within the cityping window, if ignores all pixels outside the window and does not generate any output for their the upper left poordinate of the cityping wintow can be a fractional value, indicating a starting column between two pixels, or a starting tow between two

The Y Scaler uses a nearest reighbor (decimation) algorithm to scate an image vertically and insintains a row index generator and an 11-bit row counter. At the beginning of each field:

- the row index generator resets to the value programmed into Registers IPU1. Yilini, and
 - the row counter resets to 1 for field 1, and to 2 for held 2 (interlaced data only)

data. The current row is output when it ties within the choped region and is within one row of the row under generator value. The row index generator value then increments by the Y shrink value programmed into The row counter determines if the current row lies within the clipped region. For each row input to the Y Registers IPU1_YSnt. This procedure repeats until the current row reaches the boundary of the clipped scaler, the row counter increments by 1 for progressive scan data, and increments by 2 for interfaced

Registers IPU1_YSnl specify the vertical scaling factor as a 6-10 lixed point strunk value. The following equation specifies how the shrink value is used:

within the clipped region, and it increments by 1 for each pixel processed by the X Scalor When the current pixel has which the clipped region and a within one pixel of the pixel with a generator value, the interpretation circuit produces an output give. The pixel wides generator value then increments by the X Shirik value specified by Registers IPU1_XSnf. This procedure repeats until the current pixel his outside the counter. At the beginning of each row, the pixel index generator resets to the value programmed into Hiry isters IPU1 XBnl, and the pixel counter resets to 1. The pixel counter determines if the current pixel has The X Scaler uses an interpolation circuit that maintains a pixel index generator and un 11 bit pixel

Registers IPU1_XSnf specify the horizontal scaling factor as a 6-10 fixed point strink value. The following equation specifies how the strink value is used:

The Frame Buffer Data Bus transports data as priet pairs. Therefore, the controlling software rightly must ensure that the Window Capping Unit and the X Scaler produce an even number of priets pur row FIFO G will not operate correctly when an odd number of pixels per row is produced. NOTE:

Special Y Scaling Path Mode

stored in the frame buller (in contrast to the decimation method). This mode is specified by field YSP in The Y Scaler works with the ALU to amplement a special two line vertical interpolation using an artitle?

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Registers IPU1 MCfff, and held AOP in Registers ALU MCfff, Sue also: ALU: Arithmetic and Logic Unit, page 63, Table 3:23, and Section 4.3.2.8 on page 109.

3.3.2.7 IPU1 Interrupt Request Unit

The IPU I contains pixel, line, and field count registers that provide input stream based interrupt requests based on any combination of line and field counts. These registers are described in Table 3.17.

Table 3-17. IPU1 Interrupt Request Unit -- Control Registers

Register	Field	Function
IPU1_PIX	1	Pixel count Register. This 11-bit upcounter is incremented as each pixel is input to the IPUT; it is automatically reset to 0 at the beginning of each line
Jan Inc	ı	Line count Register. This 11-bit upcounter is incremented at the beginning of each line input to the IPU1, it is automatically reset to 0 at the beginning of each held its LSb specifies the held ID for interaced sources; 0 - held 1, 1 - held 2.
IPUI_FLC	1	Field count Register. This 16-bit upcounter is incremented at the beginning of each held input to the IPU1. Unitie the parel and his counters, the held counter can be reset under software control (see Register IPU1_ETR below).
เคบา	l	Line Count Interrupt Request. Specifies the 11-bit line count value at which an mismupt request should be generated.
PUI FIR	1	Field Count interrupt Request. Specifies the 16-bit held count value at which an interrupt request should be generated. While bit 15 of this register = 0, Field Count Repsire I PULT. FLC is hand as a count of 0.5ee Section 4.1.5 for more information on the interrupt request system of the CL 9220,h.

3.3.2.8 Output Format Converter Unit

The Output Format Converter Unit packs the 25 bit video stream used exclusively within the IPU1 into the pixel pair format used by the internal Frame Buller. Data Bus and the Frame Buller. It does not perform color space conversion. It supports the output formats shown in Table 3-18.

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Table 3-18. Frame Buffer Data Formats

NOTE: These formats are shown for consecutive input pixels a d

	2		2						
Frame Buffer Bit	A:2:2 Non- tagged	4:2:2 Tagged	5:5:5 Non- tagged	5:5:5 Non- Tagged	5:5:5 Tagged	8.8.8 Non- Tagged	8:8:8 7:00ed	3:3:2 16-bit	3.3.2 32.bit
FB031	4,7	47.b	4/B	1	l	:	-	,	147
FBD30	¥6,	∀ 6	P.	H,	Ë	:	• i	1	<u>چ</u>
£8029	×°	×S.	£	8	چ	,	:	:	
f B028	¥	¥.	ž	ş	ŝ		:	;	ີ ວັ
FBD27	۲,	۲,	독	ž	ź		•	ì	2
£8026	¥2°	Y28	ć	Ę	Ę	ı	•	,	Š
FB025	۶	۲.	ජි	g,	2	:			`.`
f B024	٥	Š	ś	Š	ર્જુ	:	:		.g
F8023	۸,	۸,	ð	Ş	ś	H,	E,	:	ž
f 8022	9	9^	පි	Š	చే	. <u>.</u>	1 9	!	<u>.</u>
F8021	%	\$^	8	ć	g		ž.	:	£
FB020	;	; ;	97,	8½	B/8	ž	ž		6
f B019		۲3	B	B6 ₆	96	3	33		<u>چ</u>
F8018	~	٧2	8	92	93°	€.	2•	•	ંદું
F8017	5	; >	8	940	64°	Ē	Ē	٠	è
FBD16	°,	مِ	68	93	9 3°	9	190		Ą
FB015	۲,۰	٧٧,	è	1	_•	6,	6,	ž	ž
FB014	4 9,	Y6	ž	A7.	`≃	ී	8	, <u>e</u>	
FBD13	, *	Y5.	AS,	1864	E	55	3	£	₹.
f B012	¥.	¥.	Ę	ns,	£	3	3	3	3
F8011	۲,	, Y3,	€	ž	ž	3	3	. 99.	ئي
FB010	¥2,	Y2.	G,	H3,	£3,	ŝ	2	ŝ	Ŝ
f B09	÷*	<u>,</u>	ප්	ç,	ŝ	• •	5	£,	ž,
FB08	o* ×	, 0,	ŝ	3	3	පී	8	156 ₈	£
FBD7	'n	'n	8	ŝ	ŝ	87,	H	≥	3
F B D 6	Š	* 5	6	3	3	90	90	9	€
6805	Š	ŝ	62	පී	3	88,	115,	₹.	£
F804	3	3	6 ′•	8 ′•	9,	94	ž	3	3
F803	ŝ	ຣິ	8	8	96,	6 0	. CH	3	હૈ
F802	°	ŝ	82	8 2	82°	8 2,	6 2	3	S.
FB01	5	5	8	6	8	B	Ξ,	≥	è
FB00	9	_	83	83	8	2	3	1	

NOTE: The controlling application software must track the format of the video stream being processed within this IPU1 and the Frame Bullet for both held lines for example, a would be invised to specify an HGH right stream with an outbut YCDC stream. The 25 bit HGB stream formed by the trout format Convertier must remain RGB data because the Output Format Convertier Unit cannot perform the color space convertier must remain RGB data because the Output Format Convertier Unit cannot perform the color space convertier an RGB output stream since the right YCDC stream would be converted with an RGB using the Color Space Convertier This data is then to RGB using the Color Space Convertier This data is the packed with the specified Hill format for use by the internal Frame Buffer Data Bus and the external Frame Buffer Data Bus and the external Frame Buffer.

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3.3.3 IPU2: Input Processor Unit 2

The IPU2, shown in Figure 3.19, prepares an input video stream for ALU processing and/or storage in the Frame Buffer. The stream is output through FIFO F.

The IPU2 has two Master Control Registers (IPU2, MCR1 and IPU2, MCR2), allowing the IPU2 to perform different operations on two independent, field synchronized, single field video steams during a common frame time. Field ID Signal FID, shown in Figure 3-19, determines the register set to be used. See also: Field Toggling and Field ID, page 42.

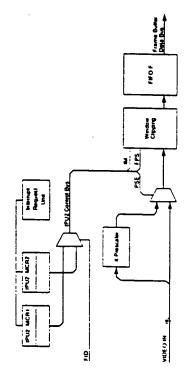


Figure 3-19, Input Processing Unit 2

The IPU2 contains three subunits, each of which is detailed in the following paragraphs:

- IPU2 X Prescaler
- IPU2 Window Clipping Unit
- IPU2 Interrupt Request Unit

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3.3.3.1 IPUZ X Prescaler

second luminance chaintel value, and every second chrominance chaintel pair values, as shown in Figure 3.20. Data along the Y axis of the input stream is unchanged. Fields PSE within Registers IPU2. MCH. The X Prescaler is a 2.1 decimator designed specifically for 4.2.2 YCbCr hybit streams. It drops every specify whether the X Prescaler is enabled or bypassed.

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Figure 3-20, IPU2 2:1 Prescale Example

3.3.3.2 IPU2 Window Clipping Unit

The Window Cipping Unit, shown in Figure 3.21, delinos the cipping window. - a rectarigular area of interest in the input wideo data stream. The cipping window can be a region of only a few pixels per side, up to the entire input stream, and is defined by the following registers:

 Registers IPU2_XEII and IPU2_YEII specify the lower right corner of the chipping window Registers IPU2_XBII and IPU2_YBII specify the upper telt corner of the chipping window.

The Frame Butler Data Bus transports data as priet pairs. Therefore, the controlling algorization software must ensure that the Window Cropping Unit produces an even number of puets per row. FH (1) it will not operate correctly if an odd number of puets per row is produced.

Table 3-19, IPU2 Window Clipping Unit — Control Registers

	interlace Mode. Specifies whether the input stream is interlaced or non-interlaced.	Field Potarity Select. Speciles the sync polarity of the input stream
Function	Interface Mode.	Fleid Potarity Se
Field	2	FPS
Register Field	PU2_MCRI	PUZ MCRI FPS

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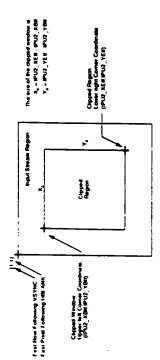


Figure 3-21. IPU2 Window Clipping Unit

3.3.3.3 IPU2 Interrupt Request Unit

The IPU2 contains Pixel, Line, and Field Count Registers, described in Table 3:20, that provide input stream based interrupt requests based on any combination of line and field counts.

Table 3-20. IPU2 Interrupt Request Unit — Control Registers

Register	Field	Function
IPU2_PIX	I	Phet count Register. This 11 bit upcounter a incremented as each pinel is upput to the IPUZ It is automatically reset to 0 at the beginning of each line
PU2_LIC	1	Line count Register. This 11 bit upcounter is incremented at the beginning of each tine input to the IPU2 it is adomatically reset to 0 at the beginning of each field. Its 5b specifies the held ID for interlaced sources: 0 = held 1, 1 = held 2.
#U2 ftc	ı	Field court Register. This 16 bit uppounter is incremented at the beginning of each held input to the IPU2. Unitie the pixel and his counters, the leid counter can be reset under software control (see Register IPU1_FIR below).
IPU2_LIH	1	Line Count interrupt Request. Specifies the 11-bit line count value at which an interrupt request should be generated
IPU2 _. FIR	ı	Field Count Interrupt Request, Species the 16 bit held count value at which an interrupt request should be generated. While bit 15 of this register = 0. Field Count Register (PUT, FLC is held at a count of 0. See Section 4.1.5 for more information on the Interrupt Request System of the CL. PX2070.

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3.3.4 ALU: Arithmetic and Logic Unit

The ALU, shown in simplified form in Figure 3.22, is actually more than its name implies. It can operate on a pixel togically or arithmetically, or replace it or one of its component values with a constant. It can decode and/or encode pixels tags. A simplified block diagram is shown below.

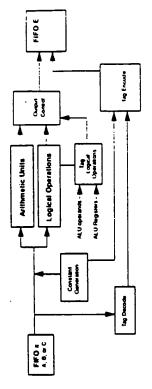


Figure 3-22. ALU Simplified Block Diagram

The ALU, shown in Figure 3.23, processes two simultaneous input video streams through Fif Os A and B, as well as the mask or mixing controls through FIFO C. Processed streams output through FIFO E

The ALU accepts the following input streams and performs the corresponding function for each

- tagged and non-tagged YCbCr arithmetic, logical, and tagging operations; tagged and non tagged RGB — logical and tagging operations
- 8-bit pseudocolor input streams togical and tagging operations.

Registers ALU, MCRI control steam format, operand source selection, tagging operation selection, and arithmetic or logical operation for both field times. Table 3:23 lists the arithmetic operations Arithmetic and logical operations are mutually exclusive during a single held time

Like most of the other VPU subunits, the ALU has dual processors. Field ID Signal f ID determines the register set to be used (refer to Section 3.2.2.2 on page 42).

The ALU has five primary functions, which are described in the following subsections

- Operand Selection
- Data Tagging
- Logical Operations
- Arithmetic Operations Output Selection.
- Section 3.3.4.6 describes the special Y Scaling Path. Refer to Figure 3.23 for all discussions of the ALU.

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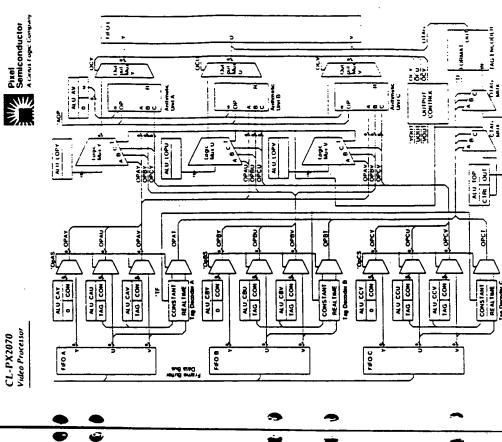
3.3.4.1 Operand Selection

The ALU contains three input FIF (1)s — A. B. and C. Data input to FIF O A sources Operand A (OpA), data input to FIF O B sources Operand B (OpB), and data input to FIF O sources Operand C (OpC). With the exception of the special Y Scaling Path and bit per-pixel controls in OpC, each input FIF O and its operand selection carcuit are identical.

YCbCr imput streams are subdivided into separate 8 bit Y, Cb, and Cr component channels. RGB input streams are subdivided into separate 8 bit R, G, and 8 component channels.

Table 3-21. Operand Selection — Control Registers

Fleid Function	Constant A, Charmels YUV. Specifies the 8 bit constant values to supply to each component charmel and the lag bit	II OPAS Operanda ABC Source Select. Specifies whether the OpA multiplearers select OPBS the real time video stream or the contents of Registers ALU_CAx as the input for OPCS the logical and/or antihinese sections. NOTE: Feld OPAS control four multipleares simultaneously: the YR, CbC, and CR component channels and the table stream data and onstand data cannot be mised in the same operand during the same held. However, for a given operand, real time stream data can be same held. However, for a given operand, real time stream data can be seen the data cannot be the constand cast ince stream data can be selected during one held. I and constand cast ince stream data can be
Flek	1	8 0 0
Register Field	AIU, CA	ALU_MCHI OP



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Figure 3-23. ALU: Arithmetic and Logic Unit

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3.3.4.2 Data Tagging

Data Lagging in the ALU performs three independent tasks:

- · Logical operation,
- output multiplexer control, and
 - output stream tag value.

The operand selection multiple rets select either the realtine lag or a constant lag as specified by the operand selection fields OPAS, OPBS, and OPCS (see Section 3.3.4.1). The control lag (CTAG) and the

Table 3-22. Data Tagging — Control Registers

Function	Operands ABC Source Select. Species that the operand selection multiples. ers select either the reatime lag or a constant lag (see Section 3.3.4.1).	Teg Formet. Specifies the format of both the input and output streams
Field	OPAS OPBS OPCS	<u>+</u>
Register Fleid	ALU_MCR	ALU MCRI TF

Specifying 'No Tag' ensures that no tag bit will be added to the output stream (see Section 4.3.5.1). However, a constant tag could be generated for one of the operations, which in turn could be used by the logical operations or output multiplexers. Similarly, one of the tagged data formats could be specified. The output lag multiplaser could be programmed to pass the rag unchanged, or override the input lag with a new value of the district countries of the strain carrot be changed. The controlling software application must lagging are consistent with the desired operation and stream format.

Logical Operation Control

the input bit to be selected from field CTC of Register ALU. TOP to generate CTAG. CTAG is one of four control signals provided to the togical operation multipleaus, and is also used by the output control section, as described in Section 3.3.4.5. Since each operand contributes a single, realitine control bit to the The lag bits from each operand are combined at the control lag multiplexer. This combination specifies CTAG multiplexer, logical operations and output selection can be controlled on a pixel by pixel basis.

in the same way, the tag bits from each operand specify the input bit to be selected by the output tag multipherer from field OTC of Register ALU. TOP to generate OTAG. OTAG is the output tag value that FIFO multipherer, the output tag can be controlled on a pixel by pixel basis.

The value of the output lag is encoded under control of the TF held in ALU_MCR, then passed to the out-

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3.3.4.3 Logical Operations

The ALU performs logical operations using eight parallel 16.1 multiplexers, each providing one bit to the 8 bit output stream. Register ALU_LOPY specifies the 16 bit liquot to all eight multiplexers

to the multiplexer. Each 16 1 multiplexer uses a different bit from each of the channel streams — the first uses bit 0 from each stream, the second uses bit 1, etc. All eight multiplexers share the CLAG value. Dit ferent operations can be programmed for each channel of the same input stream. The CTAG control and eight bits from each channel of oach operand provide a 4 bit input selection control

3.3.4.4 Arithmetic Operations

The arithmetic sections of the ALU only process YCbCr input streams. They do not support RGB streams The arithmetic unit performs eight operations, as shown in Table 3.23

Table 3-23. Arithmetic Operations

NOTE: U = unsigned 8 bit (Uses excess 128 notation where appropriate. See also 3.3.2.3, puge 54.)

Function	Alpha mir using ALU AV	Alpha min using C	Add A and B	Subtract B from A	Ofference A to B	Reconstruct from A and H	Four frame interpotate from A and B	Special At IV Scaling Path
Op.A. OpB OpC E Formula	- U E • (A'a) • (B'(1 u))	U U E • (A'C) • (B'(1·C))	U E-A.B	- U E.A.B	E - (A · B) / 2	E - A . (2'8)	E - A . ((2'8) / 4)	- U E - (A'n*) + (B'(1-n))
E	5	>	>	-	s	 	5	5
Opc	ı	o l		1	,	1		,
900	5	2	,	_	_		,	
¥d0	5	ם	5	כו	5	ם	3	ם

a n - hactional pixel value from IPUZ scaler

Table 3-24. Arithmetic Operations — Control Registers

ALU_AV — Aphie value, Specified mix value when performing a constant appra	Register Field	Field	Function
-	ALU_MCRI	AOP	Allhmetic Operation Select. Specify the arithmetic operation to perform for each held time.
	ALU_AV	-	Alpha value. Specifies the aprila mix value when performing a constant signal mix.

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3.3.4.5 Output Selection

The output multiplexers select between the output of the logical operation multiplexers and the arithmetic und CTAG and fields YOUT, UOUT, and VOUT of Registers ALU MCRt specify the output selection of each output multiplexer. Since CTAG is generated by the reatime input steam, output selection can be

3.3.4.6 Special G-Mixed Y Scaling Mode

polation scales in the Y direction using a table of Ct values (as opposed to the decimation method). Fields The Y scaler, in combination with the ALU, provides a special mode of operation in which a 2-line inter-YSP in Registers IPU1_MCRI and field AOP in Registers ALU_MCRI specify this mode (see Section 3.3.2.6 on page 56).

3.3.5 OPU: Output Processor Unit

The OPU, shown in Figure 3.24, converts the stream data written to FIFO D from the format used in the Frame Butler to an output stream format. The OPU contains three subunits, each of which is detailed in the following paragraphs:

- Output Format Converter 2:1 X Zoom Unit
- OPU Window Cipping Unit.

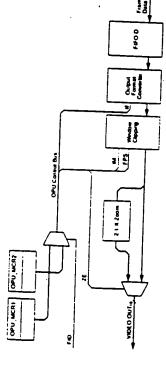


Figure 3-24, OPU: Output Processor Unit

allowing the OPU to perform different operations on two independent, single-field video streams during a common frame time. Field ID Signal FID determines the register set to be used. See also: Field Toggling The OPU has two Master Control Registers (OPU , MCR1 and OPU , MCR2) — one for each field time and Field ID, page 42). MOTE

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The Frame Bufler Data Bus transports data as pirel pars. Therefore, the controlling application software must ensure that EFFO D receives an even number of pirets per low. EFFO D will not operate correctly at it acterives an odd number of pirets per row.

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Video Processor



3.3.5.1 Output Format Converter

The Output Formal Converter unpacks the pixel pair stream data written to FIFO D into one of tive formals for bansport to the VRU. The OPU supports two YCDCr and three RGB formals The OPU supports two YCbCr and three RGB formats (refer to Table 3.14, Table 3.15, Table 3.16, and

- YCbCr 4:2:2 non-tagged
- YCbCr 4:2:2 tagged
- RGB 5:6:5 non-tagged
 - RGB 5.5:5 tagged
- RGB 3:3:2 non-tagged.

NOTE: The OPU does not convert between YCDCs and RGB formals. The controlling software application must track the format of the video stream transported from the firame Buller to the OHUTor both held times for example, it would be invalid to specify an RGB output stream if the Frame Buller is actually supplying a YCDC stream.

3.3.5.2 2:1 X Zoom Unit

exactly twice the number of pixels input. A linear interpolation unit generates a new pixel with a value av The 2:1 X Zoom Unit performs a 2:10:1 zoom atong the X axis of the output stream. That is, it outputs erage that of the pixels on either side.

The 2:1 X Zoom Unit does not support RGB 3.3.2 non lagged output streams

3.3.5.3 OPU Window Clipping Unit

The Window Clipping Unit defines the chipping window — a rectangular area of interest in this stream bransported from the Frame Buffer Data Bus. The chipping window can be a region of only a few pixels purside, up to the entire input stream, and is defined by the following registers

- Registers OPU_XBII and OPU_YBII specify the upper left corner of the chipping window.
- Registers OPU_XBit and OPU_YEtt specify the tower right corner of the chipping wrindow

Jable 3-25. OPU Window Clipping Unil — Control Registers

Function

Field

Register

OPU_MCRI	3	brierlace Mode. Specifies whether the urpul stream is mitelaced or non-inter- taced.
OPU MCRI FPS	FPS	Field Polarity Select. Specifies the sync polarity of the input stream

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3.4 RFU: Reference Frame Unit

The RFU, shown in Figure 3.25, creates and manages multiple reterence frames, and provides simulta

neous access to eight other bullers and four display windows.

The RFU contains three suburils, each of which is detailed in the following sections:

The OBU and DWU Registers control the operation of the RFU.

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MMU: Memory Management Unit.

 DWU: Display Window Unit OBU: Object Buffer Unit

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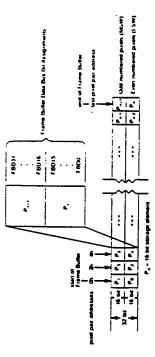


Figure 3-26. Frame Buffer Addressing (32-bit)

The Linear Slart Address (LSA) represents the upper-left corner (coordinate (0,0)) of the reference frame It specifies the start of the reference frame relative to the start of the Frame Buriter (physical address

Bose of the second

13

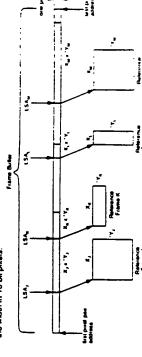
Address generators controlled by object and duping windows MMC

ž ÇAS. NOTE: The CL PX2070 does not specify a height parameter when defining a reference frame. The controlling software application must ensure that the object buffers and display windows are boated within the intended boundaries.

The linear addressing architecture of the RFU altows reference frames to be affocated from configuous. one-dimensional strings of memory, rather than inefficient rectangular areas typical in singiler archited tures. A reference frame is specified by two values, as shown in Figure 3.27

· the LSA, and

· the width in 16 bit pixels.



not programmed exto the CL Pa2070 "Denember must be empleed by the controlling software

Figure 3-27. Reference Frame Allocation

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Figure 3-25. The Reference Frame Unit

deallocated as necessary by the controlling software application, they can be any size, order, or location, Reference frames are rectangular, two dimensional regions of the Frame Buffer that are affocated and

The name reference frame comes from the manner by which the RFU manages the frame buffer. Rather than re-arranging graphics objects by recopying bitmaps, the CL. PXRO70 moves the frame of reference around the data that represents the object. A number of virtual frame buffers can exist within the physical

NOTE: The number of writtal reference frames which can be allocated is limited only by the folial amount of mem-ony available in the Frame Buffer. However, there can be no more than eight physical, simultaneous ref-erence frames (since the CL-PX2070 contains only eight object buffer register sets).

The RFU accesses the Frame Buttor using linear rather than rectangular addresses, as shown in Figure 3-26. Although all storage elements are 16 bits wide, the Frame Butter is addressable only on 32-bit, or prial pair, boundaries; therefore, the LSb of the address is always treated as 0h, regardless of the value FBU[31:0] are controlling software application. The bit assignments used by the Frame Buffer Data Bus



3.4.1 OBU: Object Buffer Unit

The OBU creates and manages up to eight physical smultaneous object bullers, each of which can be programmed (via its knear start address; or LSA) to be located anywhere in the frame buffer memory. The object buffer, shown in Figure 3.2e is a rectangular, two dimensional storage repon allocated within a reterence frame. The object buffer is the only means by which data can be stored to or retrieved from

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- Obto AFI		ть'х).		Object Buller N	Phones
	15A 1900_(154)	i g		Š	į
*	Open Brie				
Reterence Frame L	(15) "0180 HS1" 9180 Offers Britan 15A				

Parameter supported by Phael Semiconductor, Inc., tow lavel directs

Figure 3-28. Object Buffer

The OBU atlows each object buffer to be locked to either video source, or to be programmed to operate independently. Object buffers also can be placed anywhere within the knearty-addressable Frame Buffer. One pair of registers for each object buffer completely specify an object buffer and locate it within a refreence frame, as shown in Table 3.26.

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Table 3-26. Object Buffers — Control Registers Function

Fletd

Register

9 00	9S7 ⁻ 9180	1	Diaglay Window Linear Start Address. Species to location of the object buffer. This physical location represents a corner of the retaingular region relative to the start of the frame Buffer (physical location 00000th), not relative to the reterence start of the frame Buffer (physical location 00000th), not relative to the reterence starts.
REXX BSX BSX BSX CS DM7-DM0 CS DM7-DM0 R Y8DC R FA R 1ME	DBU ₀ _MCR	XBDC, YBDC	XY BLT Direction Conitrol. Determine which corner of the object buffer is speci- hed.
BSX BSX BSY RSVD LSL SN OPM OPM A YBOC YBOC YBOC YBOC YBOC YBOC YBOC YBOC	OBU6_RFX		Object Buffer Reference Frame X Size. Speches the X dimension (pikh) of the reference train an 16 but pixets OBLIO, RFX is the only OBLI Register that has any direct, hardware control of the reference kame.
BSX BSY FSV 1 (St 1 (St	08Uo_8Sa	1	Object Butter Size. Specifies the X and Y dimensions of the object buffer in 16 Dri priets.
BSX BSY RSVD LISL DM7-DM0 OPM VBDC YBDC YBDC YBDC FA	OBU _B RFX	RFX	the X demension of the reference frame, within which the object buffer is relatively tocated (the Y dimension is implied by number of linds).
RSVD LSL OPM OPM YBDC YBDC YBDC YBDC	OBUG BSX OBUG BSY	BSX BSY	She X and Y size of the object;
OPM OPM OPM YBDC YBDC FA	751 9180 0800 1.5H	RSVD	the standing pixel of the object buffer.
OPM XBDC YBDC YBDC IME	080e_0EC	DM7-DM0	output decimation — small preview windows which can be displayed at low band width.
YBDC YBDC YBDC	OBUN MCR	OPIM	operating mode.
FA	OBUL MCR	XBDC	X and Y But directions:
LME	OBUS MCR	3	FIFO association.
CME	OBU6_MCR	CNE	chominance and luminance channel masking

An object resize operation illustrates the advantages of this arrangement — the procussor must only write to those registers to complete the resizing. "Tearing" is eliminated by only moving" during the Vsync time.

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Table 3-28. DWU: Disptay Window Unit -- Control Registers (cont.)

Function Field Register

Otaplay Window Display Y Start, Specials the number of rows between the top row of the CRT display and the top row of the display window.	Display Window Horizontal Control Register. Species the total number of active priests per row appeted by the current sync parameters of the output CR1 Ospiay device (The number of rows to output is not required.)	Functional only when used with Ct. PX2080. Specifies zoom factor. The image is scaled accounting to the following formula:
1	ł	Y200M. X200M
DWUM_DSY	DWU_HCR	DWUG DZF

Scaling . ZINCHA EACTUR

Operation with and without the CL.PX2080 MediaDAC**

The CL PX2080 MediaDAC is a companion device for the CL PX2070 that allows overlapping (occluded) display windows, as specified by field OCC in Register DWU_MCR.

- When the CL. PX2070 is used with the CL PX2080, the system supports up to four occluded display
 - When the CL. PX2070 is used without the CL. PX2080, the display windows cannot overlap. In this case, the controlling software application must ensure that:
 - - the display windows do not overlap;
- adjacent display windows are separated by the minimum distance specified by Register DWU_HCR.
 - rows within a display window do not cross physical memory row boundaries.
- The value written into Register DWU HCR depends upon the dosclock of the CRT display system. For more information, see 4.4.3.2, page 147. Use the following equation to determine the minimum possible. NOTE

MWS . GPCLK penud

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3.4.4 MMU: Memory Management Unit

The MMU provides ORAM/VRAM support and translates the parameters from the rest of the system into physical memory addresses using Register MMU "MCR, as shown in Table 3-29. Frame buffer size can be up to 8 megabytes.

Table 3-29. MMU: Memory Management Unit — Control Registers

Function

탈

Register

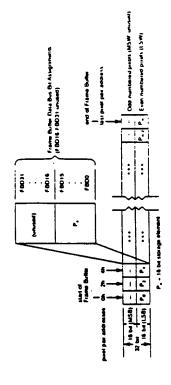


Figure 3-31, Frame Buffer Addressing (16-Bit)

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3.4.4.1 Frame Buffer Architecture

The frame buffer is a DRAMAYRAM array with a 3.2 bit data bus (FBD[31 0]). Two RAS' signals are provided to select between two 3.2 bit banks. Four CAS' signals are provided, and are hypically used for byte selection. The memory device size is chosen from the options in field FBC of the MMU. MCR register, described in Section 4.4.2.1 on page 145. Figure 3.32 shows a typical frame buffer implementation.

FBD(31.0) FB0 FB0 [23:16] FBD [31:24] FRAME BUFFER MEMORY ARRAY BAMK I **7** <u>.</u> BANK 0 CAS1. HASI. RASO. CASO. CL-PX2070

Figure 3-32. Typical Frame Buffer Implementation

Video Processor CL-PX2070

4. DETAILED REGISTER DESCRIPTONS

This section lists and defines the CL. PX2070 registers. The registers are organized according to CL.PX2070 subsection.

MOTE: Register names containing lower case variables represent groups of registers with similar functions. For example, VII, DPC/represents both Datapath Control registers -- VIU, DPC/r (Batapath Control Field 1) and VIU_DPC/2 (Batapath Control Field 2). Table 4-1 hasts and defines all variables used in this mainton

in order to maintain compatibility with future Priet Semiconductor products, all reserved bits in all registers must be written as zero.

Table 4-1. Variables Used in Register Names

>	Variable	Replaces	\$	Variable	Replaces
١.	e (aus)	х, ч	c	n (number)	F (Fraction) or I (friteger)
ء ا	(plue)	L (Low) or H (High)	٥	o (object buffer #)	0 /
ں ا	(color space)	Y. U. V or R. G. B	۵	p (pod)	1.2
9	(display window #)	03	•	\$ (Stb4)	031
۱_	(field)	1.2	-	(channel)	V.U.Y

4.1 HIU: Host Interface Unit - Registers

Table 4-2. HIU Register Address Map

0

Register	Pat Me	Sec.	Pri. Sec. Register Map Map Definition	Used by Registers	legisters	Ref. Section
0 ⁻ UIH	27C0	0530	27C0 0290 Register VO Address 0	HILU CSU HILU DBG HILU_DRD	HIU CSU Configuration Setup HIU DBG Debug Control HIU_DRO Debug Read	4 1 1 page 62 4 1 2 page 63 4 1 3 page 64
r_UBH	27/2	0292	27C2 0292 Register IVO Address 1	HIU OCS	HIU OCS Operation Control/Status HIU IRO Interrupt Request	4 1 4, page 85 4 1 5, page 86
HIU.2	27C4	0294	27C4 0294 Register I/O Address 2	HILL RIN	HIU RIN Register Index	4 1 6, page 8/
C_UP+	27C6	9628	27C6 0296 Register I/O Address 3	HBU_RDT	HIU RDT Register Data Poil	4 1 7, page 88
¥.U.	2)CB	9620	27C8 0298 Register FO Address 4	HILL MDT	٠,	4 1 6 page 68

Table 4-3. HIU Registers Accessed by the Register Data Port

Ref. Section	4 1 9, page 88	4 1 10 purpe 89
Definition	Indexed Memory Data (Local Hardware Inter 4-19, page 88 face Mode)	Interuol Selvp
Index	0000	1000
Register	HIU_IMD	HIU, ISU

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4.1.1 MIU_CSU: Configuration Setup (Read Only)

VO Address 27C0 (Primary Map) 0290 (Secondary Mep)

Register HIU, CSU stores hardware configuration data for the CL. PX2070. An external configuration register must provide configuration data to the LSB of HIU_CSU during the reset interval. HIU_CSU is shadowed by registers HIU_DBG and HIU_DRD. Section 3.1.1 on page 27 See also.

						-	
PAS.	٥				ė	<u> </u>	ż
181	-				50	Deli :	100 130
RSVO	~				28	E .	a a
	•				. c	1 ts	88 0.0 8.0 8.0 8.0 8.0 8.0 8.0 8.0 8.0 8.0
HS8	•				abon.	of host	addre.
	•			<u> </u>	NC.	ice de	20
	•			Version	ISA an	A dies by an and a dies by an	Re- Cossen Parelec
HSVD	 		60 58	Video Processor Device Version 0000 Ct PX2070	Reserved (read as 0 in ISA and MCA modes, read as 1 in local hard-ware interface mode)	Host System Bus. Specifies the type of host system connected to the CL PX2010 CL PX2010 CL PX2010 OL MACA bus definition 100 MacA bus definition 101 MacA bus definition 101 MacA bus definition 101 MacA bus definition 101 MacA bus definition 102 MacA bus definition 103 MacA bus definition 104 MacA bus definition 105 MacA bus definition 106 MacA bus definition 107 MacA bus definition 108 MacA bus definition 108 MacA bus definition 108 MacA bus definition 108 MacA bus definition 109 M	Frame Buffer Jumper State. O DRAM 1 VIRAM Port Address Select Specifies the I/O address map that the host system should use when accessing the CL PX2070. O Primary port map select.
	•		De e	rocessor De CL PX2070	race m	stem Bus 070 1SA bus d Aur ISA MCA bus MCA bus Aur MCA Preserved Local ha	DRAM VITAM VITAM Gress Se Wd use
	•		Reserved (read as 0)	Video Pro	Reserved (read as 0 ware interface mode)	Host System Bus SS CL-PX2070 000 Aus Aba delin 000 Aus Aba delin 001 MCA bus del 010 Reserved 011 It Local harden 11x All other cord Reserved (read as 1)	Addre
VER	٥	iptor		3 8		CL 10 000 1000 1000 1000 1000 1001 1001	£ o - & € o .
	=	Description	RSVO	VER	RSVD	HSB HSVD	FBT
-	2	Access Reset	0000	000	8	Ē	
2	2		•			-	- 0
ASV02	2	Acci	Œ	Œ	Œ	c c	æ æ
	2	911	15 12	• =	9 /	5.3	- 0

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4.1.2 HIV_DBG: Debug Control (Write Only)

VO Address 27C0 (Primary Map) 0290 (Secondary Map)

Register HIU DBG controls the diagnostic mode of the CL PX2070 Field MDE of register HIU OCS must be set to 1 before write access to this register is enabled. HIU OUG is shadowed by register HIU_DRD. Field DRE must be set to 1 before read access to register HIU_DRD is enabled.

		ž	RSVD			ORE	δ	ORS	SSE	-		LE SIMOP	į	
15	:	5	14 13 12	Ξ	9	•	•	^	9	\$ •	-	2	-	•
]]		6										
9 119	¥Č		Access Mesel Description	3	ndua	5						١		١
15:10	15:10 RW	>	8	SE	9	Reserve	60) Pd (189	RSVD Reserved (read as 0)						

15:10	₹	£	HSVD	Reserved (read as 0)
	3	0	ORE	2 ∶
2:8	3	8	ORS	3
٠	3	0	SSE	ğ
5	3	•	#	Execution Enable Controls the operation of the SIU in debug mode 0 Hart CL.PX2070 . Execute instruction (auto reset on breakpoint or single step)
0.	3	8	SMABP	Sequence Instruction Memor des at which SRJ esecution w

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4.1.3 MIU_DRD: Debug Read (Read Only)

VO Address 27C0 (Primary Map) 0290 (Secondary Map)

See also.

HIU, DBG Debug Control (Write Only), p. 63 HIU OCS Operation Control/Status (Read/Write), p. 65 SRJ, McR Master Control, p. 124 SRJs_SIM Sequencer tristruction Memory, p. 127

Register HIU_DRD accesses diagnostic information provided by the global Error Delection Trap, the current object butler counters, and the StU current index. HIU_DRD is a shadow register to HIU_CSU. Field MDE of register HIU_DCS and field DRE of register HIU_DRG must be set to 1 before read access to this register is enabled.

HAND	9 4 3 5		Error Detection Trap. This held is the logical OR of all FIFO overflow and underflow lags, and the watchdog teneout. O. No error. 1. Error detected.	Upper 5 bits of X Counter (Single Step Mode) (0-1Fh)	Upper 5 bits of Y Counter (Single Step Mode) (0: 1Fh)	Sequence Instruction Memory Current Index (0.15%)
ž			ror Detection Trap Tr d underflow (tags, and No error Error detected	oper 5 bits of X Counte	per 5 bits of Y Counte	quence instruction Me
	2	Access Reset Description	EDT Er		5	SIMIN Se
, v	- 21	i i		×	Ž	S
	13 12 11 10		0	ક	ક	6
		Acc	Œ	Œ	Œ	Œ
EOI	<u>.</u>	100	5	2	9.5	•

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4.1.4 HIU_OCS: Operation Control/Status (Read/Write)

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VO Address 27C2N(Primary Map) 0292 (Secondary Map)

Register HIU_OCS controls the operating mode of the CL PX20.10 and provides status indicators. HIIU_OCS is shadowed during read cycles by register HIU_HO (see field SRC below).

-	_	_	_
			0
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	<u>.</u>	1	~
		-	_
	£	1	•
	ÇME	-	s
:	Î		•
	PEC		^
İ	T DC	Ī	•
	DPC	-	•
	MOE	Ì	2
	SRC	Ì	=
	ASVO FFH FOH DMAW SRC MOE DPC MPC DMC UMP ONE SH		2
	<u>10</u>		2
	FFH		13
	RSVD		5
	_	-	_

Access Reset Description

811 **6**

2 7 2 2 =	C C C C S	0000	FFH FDH OMAW	Reserved (read as 0) FIFO Fhall full when read as 1 FIFO D hall full when read as 1 indicates DMA was state when read as 1 Status Read Select. Specifies register to access during a read cycle.
_ _	10 W	• •	NOE NOE	Status Head Seeds Opermas register to access during a read cycle of the dead status from register to CCS. 1 Read status from stadow register HIU HIQ Master Debug Enable Controls access to the debug support registers 0 Disable debug operation. 1 Enable debug operation. enables access to registers HIU. 0 86 and HIU. 080
	PW PW	•	MPC	Ospalay Window Posting Operation Conitol (auto resel). Specifies the register posting mode of the UNU. 1. Exable posting. 1. Exable posting. Master Posting Conitol (auto reset). Enables or disables all register posting oper of the CLP RZQV. 1. Exable posting. 1. Enable posting.
	¥	0	PMC	Possing Mode Control Specifies normal register positing or furces an immediate register posting operation 0. Normal posting operation 1. Immediate post all registers (auto reset on post)
	ş	0	OMO	DMA Direction 0 DMA input to Ct. PX20/0 1 DMA output hom Ct. PX20/0
	P.W.	0	DIME	DMA Enable 0 Disable DMA transfers 1 Enable DMA transfers

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4 IVW 0 SII Soli Resel (autoressi) Causes a soli resel to be performed on all histories units. All registers are resel to 0, all fiff Os are cleared, and all counters are sel to 0 output signals are not placed initiatise 0 No resel performed 1 Perform soli resel (auto resel) 1 Perform soli resel (auto resel) 10 fiVW 0000 If M IEM. Interupt Enable Mask This held enables or disables interupt requests from the four major interupt sources. When more reduced to the requests are ORed-ary source can assert RRO See Section 4 to 0 no page 89 for additional information on the interrupt system. 1000 Enable wardhood to generate signal RO 0010 Enable wardhood to generate signal RO 0100 Enable fifth customs.	Bii e	Bit # Access Reset Description (cont.)	Reset	Descrip	otton	(cont)
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	•	MA	0	Sri	Sn	Soft Reset (auto reset) Causes a soft reset to be performed on all bremain units. As registers are caset to 0, as IFFOS are Cleared, and all contriers are set in 0. Out-off some seconds.
fUW 0000 IF IA		1			۰-	placed in instale No reset performed Perform soft reset (auto reset)
	0	¥4	0000	2	A.	interrupt Enable Mask. This held enables or disables interrupt requests from the four major interrupt sources. When more than one interrupt source is enabled, the requests are ORadiany source has master BIO. See Section 4.1.10 on page 69 for pathons and contracts.
					0000	

4.1.5 HIU_IRQ: Interrupt Request (Read Only)

27C2 (Primary Map) In Address

0292 (Secondary Map)

HIU OCS Operation Control/Status (Read/Write), p. 85 HIU ISU Interrupt Setup, p. 89 See also

Register HtU 1RQ accesses all interrupt requests generated by the IPU1, the IPU2, the OBU, the Watch dog Timer, and the FIFO overflow and underflow flags. An interrupt service routine typically uses. HIU IRO to determine the interrupt request source(s). HIU IRO shadows register HIU, OCS. Field SRC of register HIU, OCS. must be set to 1 before access to this register is enabled. An Interrupt request appears as a 1, and inactive interrupt sources remain at 0.

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			2	7	
		1	2	i	
			=	1	
			÷		

Access Resel Description 916

NSVD Reserved (read as 0)	OB 1 Object Buller Termination (auto reset on read) Indicates that an object buller termination condition occursed in the OBU	0 IFPC IFVZ Counter (auto resot on read) Indicates that a line, or vertical sync pulse interrupt request occurred in the IPUZ.	1) (4) 0 IFTC ITUT Counter (auto reset on read). Indicates that a line, held, or vertical syric pulse interupt request occurred in the IPU.	H 0 FITO Underflow (anno reset on read) indicates that an underflow condition occurred in a FITO (SIU FCS FIFO Control/Status, p. 124.)
USVD	180	DZ4I	IPIC	N I
£	0	0	0	0
15.6 R		-	σ	æ
15.6	٠ .	•		^

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Walchdog Timer to generate signal IRIO (auto reset on read). Indicates that a timeout condition occurred in the Walchdog Timer. (VIL). Will: Walchdog Timer. (VIL). FIFO Overflow (auto reset on read) Indicates that an overflow condition occurred in a FIFO (SIU FCS FIFO Control/Status, p. 124.) Access Reset Description (cont.) WDT õ 0 Œ

4.1.6 HIU_RIN: Register Index (Read/Write)

27C4 (Primary Map) MO Address

0294 (Secondary Map)

HIU_IMD: Indexed Memory Data (Local Hardware Interface Mode), p. 88 See also:

Register HIU, RIN specifies the index value of the next register to be accessed. An optional control auto-matically increments the index address on consecutive access (read or write) cycles.

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ت	14 13 12 11 10 9		Ξ	ō	•	•		٠	•	6 . 8	\vdash	-	2 0 0	$\overline{}$	· c	
100	Bit # Access Resel Description	Ross	ě	criptic	Ę	- 1										
5	₹	£	AC		Automatic Increment Control Controls the automatic increment feature of the index address 0 Daable automatic increment 1 Enable automatic increment	tic Increder ad Disabile Enable	ement : dress a auton	tic Increment Control Control der address Disable automatic increment Enable automatic increment	Cont	i sio		ge wa	2	F-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0-0	ie ait	ē
0	P.W	8	E		Register Index (0.7FFFh)	a pud	(0.77	1	!	!	!				:	:

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4.1.7 HIU_RDT: Register Data Port

IXU Address 27C6 (Primary Map) 0296 (Secondary Map)

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;			0 1 2 1 0	•
Bit 6	Access	Reset	Bit # Access Reset Description	
20	150 RW	£	DIO Register Data I/O	
	HIU MDT:	Memory	1.8 HIU_MDT: Memory Data Port (Read/Write)	
4	0.444	,		

27C8 (Primary Map) 0298 (Secondary Map) NO Address

UO port HIU MDT accesses the Frame Buffer. To maintain data integrity when reading or writing to this port, first check the status of the appropriate FIFO.

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	13 12 11 10 19 10 1 1 1 1 1 1 1 1 1 1 1 1 1 1	_
	<u> </u>	2

	Memory Data I/O	4.1.9 HIU IMD: Indexed Memory Data (Local Hardware Interface Mode)		
	MIO	Memory D		
	£	D: Indexed	A Address HILL FILL	000
	₹	₹	ess	•
:	15.0	4.1.9	M) Add	Inde

Register HIU_IMD may be used to accesses the Frame Gulfer when the CL PX2070 is operaling in local hardware interface mode. The CL PX2070 accesses the Frame Buller through register HIL IMD is specified.

	_	
15 14 13 17 11 10 9 0 7 6 5 4 3 2 1 0	Bit # Access Resel Description	15.0 fbw on MiO Memory Data I/O
		:

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CI.-FX2070 Video Processor



4.1.10 HIV_ISU: Interrupt Setup

I/O Address HIU RDT

Register HIU, ISU specifies the interrupt modes for the IPU1. IPU2, and the OBU Any interrupt requests generated in the IPU1, IPU2, and OBU must also be enabled through field IEM of egister HIU, OC.S IPU interrupts are combined with an AND function. If more than one interrupt source is enabled within an IPnS field, all sources must be active before an interrupt request is posted.

The interrupt sources in the OBIS held use an OR function. If more than one interrupt source is selected,

any one active source can trigger an interrupt.

ASVD 15 14
ASVD 1 1

	Access Reset	Reset		
15.14	P.	8	ASVD) Reserved (read as 0)
13-11	P.W	90	IP2S	IPUZ Interupt Select. Specifies the IPUZ fine count, field count, and in pud vertical sync pudse combination required to generate an interrupt re quest. 901 Interrupt on fine count. 100 Interrupt on VS ync.
901	RW	000	S14	PU1 interrupt Select Specifies the IPU1 incount, held count, and in put vertical sync pulse combination required to generate an interrupt is 001 interrupt on his count 000 interrupt on held count 100 interrupt on NSync.
0 .	A.W.	5	Sign	Object Buffer Termination Interrupt Request. Specifies the ORU object buffer fermination conditions combination required to generate an interrupt request sognal IRO. In Object buffer of termination of the Object buffer of termination of the Object buffer a termination of Object buffer and Object buffer a termination of Object buffer a ter

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4.2 VBU: Video Bus Unit -- Registers

Table 4.4. VBU Registers Accessed by the Register Data Port

Register	Index	Definition	Ref. Section
ideo Int	VIU: Video Interface Unit		4.2 1, page 91
VIU. INCRI	1000	Master Control VI	4 2.1.1, page 91
VIU MCR2	1001	Masier Control V2	4.2.1 1, page 91
VIU DPC1	1002	Datapath Control Field 1	42.1.2, pege 92
VIU, DIPC2	1001	Datapath Control Field 2	4 2.1 2, DBOB 92
VIU, WDT	1001	Watchdog Timer	1213 0000 01

VSU: Video Sync Unit	nc Unit		4 2 2, page 95
VSU HSW	1100	Honzontal Sync Width	4 2 2.1, 0409 96
VSU HAD	101	Honzontal Active Delay	4 2 2 2, page 96
/SU HAP	1102	Honzontal Active Pixels	4 2 2.3, page 97
VSU HP	1103		4224, page 97
vsu vsw	104	>	4 2 2.5, page 98
VSU VAD	!		422 6. Dage 96
VSU VAP	106	VSIJ VAP 1106 Ventcal Active Pirels	4227, page 99
VSU VP 1107	1107	Vertical Period	4228 0000 80

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4.2.1 VIU: Video Interface Unit

I/O Address HIU_RDT 1000 (VIU, MCR1 Master Control V1) 1001 (VIU_MCR2 Master Control V2) 4.2.1.1 VIU_MCRp: Master Control

Registers VIU_MCR1 and VIU_MCR2 specify the functional and I/O characteristics of Video Fort Inter faces 1 and 2.

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	ē	•	~	
į	181	i	^	
	BISP	1	•	
	IVSP		s	į
į	ISS	i	•	
į	OVSP CHISP OBP (181 IFP ISS IVSP INSP IBP 181		^	
	180	i	•	
	480	1	•	1
	OHISP	ĺ	9	
	OVSP		Ξ	
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Description	
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Access	
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	-			
5	₽v₩	0	STM	Staff Mode 0 staff mode disabled 1 staff mode enabled
=	₽VB	•	d de	Output Video Fraid Potanty 0 normal potanty 1 invested potanty
21 63	13 12 RAW	8	sso	:
=	B/W	•	OVSP	.
9	8	•	OHS D	
-	P.W.	•	dB 0	2 5
	PAW	•	8	Output Video Blank Type. Specifies type of horizontal/composes blanking signals VIBI (VRJ MCR2) when used as output? O Hilland Commission of
	RVM	•	d <u>a</u>	

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Bit & Access Res Description (cont.)

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layor Video Horizontal Sync Polamy. Specifies polamy of horizontal sync signals VIIIS (VN) MCR1) and V2HS (VN), MCR2) when used as inputs. hour Video Blank Tipe. Specifies tipe of horizontal-composite blanking signals VIBI (VIU. MCR2) when used as legans InputOutbut Mode Specifies whether Video Part 1 of V2 is input only, our input only, or displaced under the control of VIPH (V1) or V2PH (V2) to house only or vIPH (V1) or V2PH (V2) to V2PH (V2) to V2PH (V2) to V2PH (V1) or V2PH (V2) to V2PH (V1) or V2PH (V2) to V2 Input Voteo Blank Polanty Specifies polanty of homonisticomposite blanking alg-nats VIBI (VII) MCR1) and V781 (VII) MCR2) when used as inputs hond Video V Sync Polarity Specifies polarity of vertical sync signals VIVS (VIU, MCR1) and VZVS (VIU, MCR2) when signals are used as input. hpud Spre Source

VIVSAAVS, VIIISAANS, VIBLAVRI ngus in CL PX2070

VIVSAAVSV, VIIISAVRIS, VIBLAVRI ougust from CL 4PX2070

I PANES Duples, output on V1PH/V2PH high Duples, output on V1PH/V2PH low active los active high active low dSA BISP SS Ş Ē **.** ; o 0 8 Š ₹ Š Š 3 ₹ 0

4.2.1.2 VIU DPCI: Datapath Contol

HU GE MO Address

1002 (VIU DPC1 Datapath Control Field 1) 1003 (VIU DPC2 Datapath Control Field 2)

Registers VIU, DPC1 and VIU, DPC2 specify the flow of stream data and the source of control sync references for the IPU1, the IPU2, and the OPU for fields 1 and 2 8 5 1 3 PV20C 6 / PUIDC 6 01 11 21 01 11 81 VSLIDC ASVO

Bil # Access Resel Description

:			
:			
			VIPII quatitéd
12 RVW 0000 RSVD Reserved (read as 0)	000 VSURC VSU Datapath Control	000 V1 sources clock	001 V1 sources clock, V1P11 qualified
USAD	VSUDC	_	-
0000	900		
15 12 PVW	ş		
15 12	6		

				On a source coor, and a source
				010 V2 sources clock
				100 MCI K/3 Immebase
				101 MCLK/6 Immebase
				110, 111 Reserved
	P.	8	PUDC	IPULDC IPUT Datapath Control Specifies the source of control sync references
,				and input stream data for the IPU i
				000 V1 sources control sync/data
				001 V1 sources control sync/data, V1P11 qualified
				010 V2 sources control sync/data
				011 V2 sources control syncodata, V2PH quathled
				100 OPU sources data, MCI K/3 HS Imebase, sync from VSU
				101 OPU sources data, MCLK/6 HS Innebase, sync from VSU
				110, 111 Reserved
5	PW	8	(PU2DC	IPU2DC IPU2 Datapath Control Specifies the source of control sync references

5	PVW	000	IPU2DC	U2DC IPU2 Dat	(PU2DC IPU2 Datapath Control Specifies the source of control sync references
				<u> </u>	and input stream data for the IPU2 000 V1 sources control syncidata
				8	V1 sources control syncodata, V1P11 quatried
				9	V2 sources control sync/data
				5	V2 sources control sync/data. V2PH quatified
				8	OPU sources data, MCLK/3ª HS timebase, sync from VSU
				5	OPU sources data, MCI K/6 HS timebase, sync from VSU
				9	BRU sources control data, no sync controls
				Ξ	Reserved
5	B/W	Ş	200	0	OPU Datageth Control Specifies the source of control sync references
?	:	}	;	5	and the destination of output stream data from the (1911)
				8	V1 sources control sync
				ē	Vt sources control sync, VIPH qualified
				000	V2 sources control sync
				5	V2 sources control sync. V2PH qualified
				5	VSU sources control sync, MCLK/3 Imehase
				<u>.</u>	VSU sources control sync, MCI K/6 timebase
				9	BRU receives data, no sync controls

a MCI.K/3 is expressed as "sequencer clock" in some other places in this document

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4.2.1.3 VIU_WDT: Wetchdog Timer

IrO Address Hitt HD1 Index 1004

Register VII J WUT controls the operation of the watchdog timer, and specifies the field loggle mode of

1 s	-
9 6	
15 14 13 12 11 10	
RSVD MAMS	

Access Reset Description

RSVD Reserved (read as 0)	Manual Mode Start Writing 0, then 1 while MFTS is programmed to 6h inhalts a lield toggle in manual mode	13.11 R/W 000 MF1S Master Feld Topgle Select Specifies the field topgle mode for the SRU. The field topgles on the teaching edge of Vsyrc.
Reser	Manu	Maste ta
RSVD	MMS Manual Mode Start inhales a field toggi	MF 1S
15 RAW 0	٥	900
Ž.	PVW	\$
5	=	::

Field bring from VI boat video Veynor Field bring from VI output video Veynor Field bring from V2 output video Veynor Field bring from walchdog temet Field bring from walchdog temet Field bring from walchdog temet Field bring from manual mode start field bring from manual mode start field bring from manual mode start 889999555

Watchrog Irmer Enable Enables or disables the operation of the watchdog timer

O Ossable walchdog timer

Finable walchdog timer IMONI W.F. ٤ 0 ₹ ₹

٥

Imeout Specifies the watchoop ameriteinal. The timebase interval is the memory clock signal MCLK prescated by a lactor of 49,152 (3 ·

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4.2.2 VSU: Video Sync Unit

The following sections describe the VSU registers, shown in Figure 4.1 and Figure 4.2

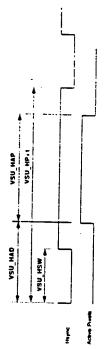


Figure 4-1, VSU Horizontal Sync Timing

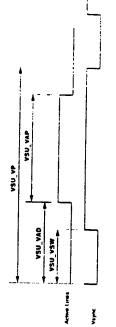


Figure 4-2. VSU Vertical Sync Timing

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4.2.2.1 VSU_NSW: Horizontal Sync Width

IN Address HILL RUL

See also

Register VSU HSW specifies the width of the horizontal sync pulse generated by the internal sync gen-	crater. The timebase is specified by helds (PU1DC and IPU2DC of register VII) DPC:
/SU HSW sp	e timebase is
Rogister V	erator Th

Figure 4.1. VSU Horizontal Sync Timing, p. 95.

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	HSW	-
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:		-
İ		2
1		15 14 13 17 11 10 9 9 9 7 6 5
:	_	=

Access Reset Description BH

		7fh)	
Reserved (read as 0)		Honzontal sync width (0 76	
USVD		IISW	
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5		Š	
15.7	!	9	

4.2.2.2 VSU_HAD: Horizontal Active Delay

FILL FILL M) Address

Figure 4.1 VSU Houzontal Sync Timing, p. 95 See also

Register VSU. HAD specifies the detay from the start of the horizontal sync pulse generated by the inter-nal sync generator to the beginning of the horizontal active interval. The timebase is specified by fleids IPU10C and IPU2DC of register VIU. DPC!

A SACRET AND ASSESSMENT OF THE PROPERTY OF THE	HAD	0 7 6 5 4 3 2 1
!		2
		=
	; }	2
	2	2
-		:
	!	ē

Access Reset Description

RSVD Reserved (read as 0)	15 10 R/W On RSVD Reserved (read as 0)
	5 E

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4.2.2.3 VSU_HAP: Horizontal Active Pixels

VO Address HIU_RDT

Figure 4.1 VSU Horizontal Sync Timing, p. 95 See also Registic VSU_HAP specifies the width of the horizontal active interval generated by the internal syncgor erator. The timebase is input memory clock signal MCLK prescaled by a factor of 3 or 6, as specified to, fields IPU10C and IPU20C of register VIU_DPCt.

		ASVD								HAP	į	AP	į		:
š	••	13	15 14 13 12 11 10 9	-	2	6	•	,	ø	\$	•	r	2	-	۰
811	Acc	888	Bit # Access Reset Description	Des.	criptic	u.									
15 11	FVW.		ક	ASV	٥	RSVD Reserved (read as 0)	od (rear	1 as 0)							
0 01	P.		£	HAP		Honzontal active priets (0 3FFh)	E SC	'e pre	IS (0 3F	Ē				 	

4.2.2.4 VSU_HP: Hortzontal Period

HIU, ROT VO Address

Figure 4-1 VSU Horizontal Sync Timing, p. 95 See also.

Register VSU_HP specifies the width of the horizontal sync period generated by the internal sync generator. Ini Immbase is input memory clock signal MCLK prescaled by a factor of 3 or 6, as specified by finitis INTEDC and IPUZDC of register VEU_DPC!

NOTE: The number entered in HP must be one less than the desired interval. See Section 3.2.3 on page 4.3 in additional information.

		¥	ASVD					j	į	4		:	:		
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ē	=	2	0 1 2 1 1 10 8 8 7 8 8 1 1 1 10	=	2	•	•	7	•	~	-	<u>-</u>	~ :		_;	c
# 16 Bit	ÞČ	8	Bit# Access Reset Description	ē	criptk	5				١		Ì	ļ			i
15 10	15 10 R/W	_	ŧ	HSV	9	Peserve	RSVD Reserved (read as 0)	() se ()						;		
06	3		ક	Ŧ	ľ	Paris 6	Desired horizontal period (0.31 Fh) - 1	Mar De	0) po	Properted (0.31 Fh) - 1	_			:		
					-		İ			The state of the s	1	į.	!-	:		:

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4.2.2.5 VSU_VSW: Vertical Sync Width

M Address HIII FIDT

Figure 4.2: VSU Vertical Sync Timing, p. 95 See also

Register VSU VSW specifies the width of the vertical sync pulse generated by the internal sync generator. The time-base is the horizontal sync interval specified by register VSU_HP

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	~
3	-
	8
	15 14 13 17 11 10 9 0 7 6
	^
	•
	٥
	2
ASVO	=
ASVO	14 13 12 11 10 9 0
	12
	2

Access Reset Description 911.0

	Fh)
Reserved (read as 0)	Vertical sync width (0.7Fh)
nSvD R	NSV
ક	5
Š	D RVW
15.7	0 9

4.2.2.6 VSU_VAD: Vertical Active Delay

I/O Address HIU RDT

Figure 4.2 VSU Vertical Sync Timing, p. 95 See also

Register VSU VAD specifies the delay from the start of the vertical sync pulse generated by the internal sync generator to the bingining of the vertical active interval. The timebase is the horizontal sync interval specified by register VSU. HP

nsvi) vao	15 14 13 17 11 10 9 6 7 6 5 4 3 2 1 0			HSVD Reserved (read as 0)	9.0 RVW Oh VA() Vertical active delay (0.3/f.h.)	
	_	ro <u>f</u>		P. S.	Vert	il in the
	10 11 21 10	Access Reset Description		RSVO	CAD	
nsvo	2	Reset		£	£	
-	1	Access	:	*	F.W	
	2	10	;	WAL 01 51	9.0	

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4.2.2.7 VSU_VAP: Vertical Active Pixels

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I/O Address HIU, RDT Index 1106

Figure 4.2 VSU Vertical Sync Timing, p. 95

See also

Register VSU, VAP specifies the width of the vertical active interval generated by the internal sync gon erator. The timebase is the horizontal sync interval specified by register VSU_HP.

		ASVO												,	
=	[=	2	15 14 13 12 11 10 9	=	9	•	•	1 1	9	i I	•	- 2 0 0	~	-	• !
	V		Bit & Access Reset Description	9	criptk	Ĕ									
2 2	15 11 PVW		£	RSV	٥	Reserve	d (read	RSVD Reserved (read as 0)							
00	10 0 PVW	1	8	۸A		/entical	active	Vertical active purets (0.71 Fh)	0.71 Fh	-					

4.2.2.8 VSU_VP: Vertical Period

I/O Address HIU_RDT 100

See also:

Figure 4.2, VSU Vertical Sync Timing, p. 95

Register VSU, VP specifies the width of the vertical sync period generated by the internal sync generator. The timebase is the horizontal sync internal specified by register VSU, HP. This register also provides the enable and single sweep controls for the internal sync generator.

SOE	SSE		RSVD							>				1	٩٧	Ì
2	=	2	13 12 11 10 9 6 7 6 5 4 3 7	Ξ	2	-	•				Н	•	•	~ :	-	• !
-	Acc	•	Bit # Access Reset Description	å	criptk	ڃ			İ			- 1	-			•
ñ	¥		•	SGE		Sync G	enera	Sync Generator Enable				i	!	i		í
_	P.W.			SSE	ĺ	eg.	Sweet writte SGE which	Surge Sweep Enable - 1 Enables single sweep mode. When his bit is written as 1, SCE resets to 0 at the end of the sweep. When SCE is set (written as 1), another single sweep occurs after which it is reset.	SGE	esets	bles single sweep moth. Where sees to 0 at the end of the sweep oc. is 1), another single sweep oc.	at the her s	end o	M the s	ween this	When sales
13 10	P.W	1	0000	PSV	0	Ser) P	RSVD Reserved (read as 0)						:	•	i
06	5		8	à		/entica	active	Vertical active count (0 751 h)	2 0	E				:	(e	# 6

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4.3 VPU: Video Processor Unit -- Registers

Table 4-5. VPU Registers Accessed by the Register Date Port

MCR 2000 MCR 2000 MCR 2000 MCR 2000 MC 2100 MC	Masser Control Masser Control	Man	поред	Definition	
Master Control Master Control Master Count Master Master Master Count Master	Master Control Master Control Master Control Master Control Field Master Control Master Control Field	PU Globa	d Control		Mer. Section
1000 Masser Control Masser Control	1000 Masser Control Masser Control	(Pi) tare			4 3 1, page 105
100 100	100 100		000	Master Control	4 3.1.1, page 105
100 Piret Count	100 Piret Count	7Ut: Input	Processor Unit 1		432 page 106
C 2107 Line Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2200 LUT RAM Base Address 2200 LUT RAM Base Address 2200 LUT RAM Data 2200 LUT RAM Data 2200 Master Control Field 2200 X Regin Integer Field 2300 X Shrinh Integer	C 2107 Line Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2104 Field Count Interrupt Request 2100 X Regin Fraction Field 4 4 4 4 4 4 4 4 4	YN PIX	2100	Priet Count	
C 2102 Freed Count Interrupt Request 1	C 2102 Freed Count Interrupt Request 1	U1 11C	2101	Line Course	4321, page 106
10	100 100	ח מכ	2102	linos and	4.3.2.2, page 106
104 Field Count Interrupt Request 2700 LUT RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Actress 107 RAM Base Control Field 1 107 RAM Base Field 1 107 RAM Bas	100 101	JI (III	2103	EURO COLL	4 3 2.3, page 107
100 100	100 100	J. F.B.	2104	Teconia marrido Heguest	4 3.2.4, page 107
101 FlAM Base Achees 101 FlAM Base Achees 102 FlAM Daa 102 FlAM Daa 103 FlAM Daa 103 FlAM Daa 103 FlAM Daa 103 FlAM Daa 103 FlAM Daa 103 FlAM Daa 103 FlAM Daa 103 FlAM DAA 103	101 FlAM Base Achees 101 FlAM Base Achees 101 FlAM Daa 101 FlAM Daa 102 102 Flad 1 102	1 188	2200	ried Countimerupi Request	4 3 2 5, page 106
10 10 10 10 10 10 10 10	10 10 10 10 10 10 10 10	911	3301	LUI HAM Base Address	4 3 2 6, page 106
1 1000 Master Control Field	1 3001 X Begin Fraction Feed 1 3002 X Begin Fraction Feed 1 3002 X Begin Fraction Feed 1 3003 X End Integer Feed 1 3004 X Shrink Fraction Feed 1 3006 X Begin Fraction Feed 1 3006 X Begin Fraction Feed 1 3009 X Shrink Fraction Feed 1 3009 X Shrink Fraction Feed 1 3009 X Shrink Fraction Feed 1 4 3006 Chroma Key VR MaxMan Fred 1 3006 Chroma Key VR MaxMan Fred 1 3006 Chroma Key VR MaxMan Fred 1 3006 Chroma Key VR MaxMan Fred 1 3006 Chroma Key VR MaxMan Fred 1 4 3100 Chroma Key VR MaxMan Fred 1 3100 Chroma Key VR MaxMan	TACO.	1033	LUT NAM Data	4 3 2 7, page 109
1000 X Begin Integer Feed 1 1000 X End Integer Feed 1 1000 X End Integer Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Integer Feed 1 1000 X Shrink Integer Feed 1 1000 X Shrink Integer Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Integer Feed 1 1000 X Shrink Integer Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Intege	1000 X Begin Integer Feed 1 1000 X End Integer Feed 1 1000 X End Integer Feed 1 1000 X Shrink Fraction Feed 1 1000 X Shrink Integer Integer 1000 X Shrink Integer Integer 1000 X Shrink Integer Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 1000 X Shrink Integer 100		2000	Master Control Field I	4 3 2 8. Date 100
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3004 X Shank Factor Feed	3003 X End Integer Feet 1	TOV.	3002	X Begin Integer Field 1	4329 Date 111
2005 X Shark Fraction Feed 1 2006 Y Begor Faction 1 eed 1 2008 Y End Integer Feed 1 2009 Y Shark Fraction 6 eed 1 2009 Y Shark Fraction 6 eed 1 2009 Y Shark Fraction 6 eed 1 2009 Y Shark Fraction 6 eed 1 2009 Y Shark Fraction 6 eed 1 2009 Y Shark Integer Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1 2000 Choma Key VR Maudian Feed 1	2006 X Shark Fraction Feed 1 1006 Y Begor Faction Feed 1 2008 Y End Integer Feed 1 2008 Y End Integer Feed 1 3009 Y Shark Integer Feed 1 3009 Y Shark Integer Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3000 Choma Key VR Maudian Feed 1 3100 Master Control Feed 2 *** *** *** ** ** ** ** ** *	A COL	3003	X End Integer Field 1	432 10 0000 010
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3002 Y Regn Integer Field 1	3002 Y Regn Integer Field 1	YBrı	3006	, Down	4 3 2,11, page 113
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1 3009 V Shrink fraction Field 1 3009 V Shrink fineger Field 1 3000 V Shrink fineger Field 1 3000 Chroma Key VR MazuMin Field 1 3000 Chroma Key VR MazuMin Field 1 3000 Chroma Key VR MazuMin Field 1 3000 Chroma Key VR MazuMin Field 1 3000 Chroma Key VR MazuMin Field 1 3000 Chroma Key VR MazuMin Field 1 3100 Master Control Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3101 Chroma Key VR MazuMin Field 2 3100 Chroma Key VR MazuMin Field 3 3100 Chroma Key VR MazuMin Field 3 3100 Chroma Key VR MazuMin Field 3 3100 Chroma Key VR MazuMin Field 3 3100 Chroma Key VR MazuMin Field 3 3100 Chroma Key VR MazuMin Field	1 3009 V Shrink Integer Field 1 3009 V Shrink Integer Field 1 3000 V Shrink Integer Field 1 3000 Chroma Key VR Mau/Min Field 1 3000 Chroma Key VR Mau/Min Field 1 3000 Chroma Key VR Mau/Min Field 1 3000 Chroma Key VR Mau/Min Field 1 3000 Chroma Key VR Mau/Min Field 1 3100 Master Control Field 2 3101 X Begin Frazion Field 2 4 4 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5 5	YFII	3008	i Diera regenti urgana i	4 3 2 12, page 114
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300b Key Function Code Feed 1 300c Chroma Key VR Max/Min Field 1 300c Chroma Key VR Max/Min Field 1 300c Chroma Key VR Max/Min Field 1 300c Chroma Key VR Max/Min Field 1 3100 Master Control Field 2	300b Rey Function Code Feed 1 300c Chroma Key Vir MaxiMan Field 1 300c Chroma Key Vir MaxiMan Field 1 300c Chroma Key Vir MaxiMan Field 1 300c Chroma Key Vir MaxiMan Field 1 3100 Master Control Field 2 3101 X Begni Fraction Field 7	184	5005	Y Shrink Fraction Field 1	4 3 2 14, page 116
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101C	3101 X Begin Fraction Field?	MCR2	3100	Master Control Fuel 2	4 3 2 16, page 117
	A Control of the Cont	210	3101	2 Page 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4 3 2 8, page 109

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Table 4-5. VPU Registers Accessed by the Register Data Port (cont.)

Name	thdex	Definition	Ref. Section
PUL XB2	3102	X Begin Integer Field 2	4 3 2 9, page 111
IPU1_XEI2	3103	X End Integer Field 2	4 3 2 10, page 112
IPU1_XSF2	3104	X Shrink Fraction Field 2	4 3 2 11, page 113
IPU1_XSI2	3105	X Shrink Integer Field 2	4 3 2 11, page 113
IPU1_YBF2	9010	Y Begin Fraction Field 2	4 3 2 12, page 114
PU1_YB12	3107	Y Begin Integer Field 2	4 3 2 12, page 114
PUI_YEI2	9010	Y End Inleger Field 2	4 3 2 13, page 115
PU1_YSF2	3109	Y Shrink Fraction Field 2	4 3 2 14, page 116
IPU1_YSI2	310a	V Stvink Integer Field 2	4 3 2 14, page 116
PUI KFC2	3196	Key Function Code Field 2	4 3 2 15, page 117
PU1 MMY2	310c	Choma Key Y/R May/Min Field 2	4 3 2 16, page 117
PU1 MMU2	3100	Choma Key U/G Mau/Min Field 2	4 3 2 16, page 117
PUI MMV2	310e	Chroma Key V/B Max/Min Field 2	4 3 2 16, page 117
PU2: Input Processor Unit 2	cessor Unit 2		4 3 3, page 119
PU2_PIX	2300	Pirel Count	4 3 3 1 page 119
PU2 LIC	2301	Lone Count	911 anen 5 f f 4

IPU2; Input Processor Unit 2	cessor Unit 2		4 3 3, page 119
IPU2 PIX	2300	Pirel Count	4 3 3 1 page 119
DUZ LIC	2301	Lime Count	4 3 3 2, page 119
PUZ_FLC	2302	Field Court	4 3 3 3, page 120
PU2_LIR	2303	Lime Count Interrupt Request	4 3 3 4, page 120
PU2_FIR	2304	Field Count Interrupt Request	4.3.35, page 121
PU2_MCR1	3200	Master Control Field 1	4 3 3 6, page 121
PU2_XBH	3202	X Begin Integer Field 1	4 3 3 7, page 122
PU2_XEI1	3203	X End Integer Fretd 1	4 3 3 8, page 122
PU2_YB11	3207	Y Begin Integer Field 1	4 3 3 9, page 173
PU2_YEII	3206	Y End Integer Field 1	4 3 3 10, page 123
PUZ MCR2	3300	Master Control Field 2	4 3 3 6, page 121
PU2 XBI2	3302	X Begin Integer Field 2	4337, page 122
PU2, XE12	1303	X End Inleger Field 2	4.3.38, page 122
PU2_YB12	3307	Y Begin Integer Field 2	4 3 3 9 page 123

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Table 4-5. VPU Registers Accessed by the Register Data Port (com)

Definition

Index

Name

3308

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CI.-PX2070 Video Proressor

Y find Integer Field 2

Ref. Section

4 3 4 2, page 124 4342, page 124 4.3 4 4, page 127

FIFO Overflow/Underflow Sequencer Instruction Memory 0

11 Control/Status Master Control

2601

SIU MCR SU ICS SrU 100

SIU: Sequencer Instruction Unit

2802

4.3 4 1, page 124 4.3.4, page 124

Video Fracessor CL-PX2070

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Table 4-5. VPU Registers Accessed by the Register Data Port (cont) 4

2017 Sequencer Instruction Memory 2.3 2018 Sequencer Instruction Memory 2.4 2019 Sequencer Instruction Memory 2.4 2010 Sequencer Instruction Memory 2.6 2010 Sequencer Instruction Memory 2.7 2010 Sequencer Instruction Memory 2.7 2010 Sequencer Instruction Memory 2.9 2010 Sequencer Instruction Memory 3.0 2011 Sequencer Instruction Memory 3.1	Name	Index	Definition	Ref. Section
2019 Sequencer Instruction Memory 24 2019 Sequencer Instruction Memory 25 2010 Sequencer Instruction Memory 26 2010 Sequencer Instruction Memory 27 2010 Sequencer Instruction Memory 29 2010 Sequencer Instruction Memory 20 2010 Sequencer Instruction Memory 20 2011 Sequencer Instruction Memory 30 2011 Sequencer Instruction Memory 31	SIU23_SIM	2017	Sequencer Instruction Memory 23	4 3 4 4, page 127
2019 Sequencer Instruction Memory 25 201b Sequencer Instruction Memory 27 201C Sequencer Instruction Memory 27 201C Sequencer Instruction Memory 27 201C Sequencer Instruction Memory 20 201C Sequencer Instruction Memory 30 2011 Sequencer Instruction Memory 30 2011 Sequencer Instruction Memory 31	SIU24_SIM	2018	Sequencer Instruction Memory 24	4 3 4 4, page 127
201b Sequencer Instruction Memory 26 201b Sequencer Instruction Memory 27 201c Sequencer Instruction Memory 20 201d Sequencer Instruction Memory 20 2010 Sequencer Instruction Memory 20 2011 Sequencer Instruction Memory 30	SrU25_SM	2019	Sequencer Instruction Memory 25	4 3 4 4, page 127
281C Sequencer Instruction Memory 27 281C Sequencer Instruction Memory 28 281d Sequencer Instruction Memory 29 2818 Sequencer Instruction Memory 30 2818 Sequencer Instruction Memory 31	SNZ6_SIM	2010	Sequencer Instruction Memory 26	4 3 4 4, page 127
2e1d Sequencer Instruction Memory 28 2e1d Sequencer Instruction Memory 29 2e1e Sequencer Instruction Memory 30 2e1f Sequencer Instruction Memory 31	SIU27 SIM	201b	Sequencer Instruction Memory 27	4344 page 127
Sequencer Instruction Memory 29 Sequencer Instruction Memory 30 Sequencer Instruction Memory 31	SIUZB_SIM	2010	Sequencer Instruction Memory 28	4 3 4 4, page 127
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C. Attimities	ALO. WITHHING SHE LOGIC UNI		
ALU,MCRI	2300	Master Control Field 1	4 3 5 1, page 128
NLU, MCR2	1062	Master Control Field 2	4.3 S.1, page 128
LU_TOP	2062	fag Operation	4.3.5.2. page 129
ינט_אא	2903	Alpha Value	4.3.5.3, page 130
10,10PY	2304	Logic Operation Channel Y	4 3 5 4, page 130
ALU_LOPU	2002	Logic Operation Channel U	4 3 5 4, page 130
ונטבע	2906	Logic Operation Channel V	4.354, page 130
ALU_CAY	2907	Constant A. Channel Y	4.355, page 131
ALU_CAU	9062	Constant A. Channel U	4 3 5 5, page 131
IU_CAV	2309	Constant A, Channel V	4 3 5 5, page 131
ALU_CBY	2809	Constant B, Channel Y	4 3 5 6, page 131
ALU_CBU	2062	Constant B, Channel U	4.356, page 131
ALU, CRV	390c	Constant B, Channel V	4 3 5 6, page 131
NU CCY	P062	Constant C, Channel Y	4 3 5 7, page 137
ארט ככט	-590e	Constant C, Channel U	4 3 5 7, page 137
ALU, CCV	2901	Constant C. Channel V	4.3.5.2, page 13.

	3:	conc	FIFO Overflow/Underflow	4 3 4 2, page 124	
SICO SIM		2e00	Sequencer Instruction Memory 0	4.3 4 4, page 127	
SRUI SIM		2e01	Sequencer Instruction Memory 1	4 3 4 4, page 127	
SIU2 SIM		2002	Sequencer Instruction Memory 2	4.3.4.4. 0808 127	
SRJ3 SIM		2e03	Sequencer Instruction Memory 3	4.34.4, 0000 127	
SRU4 SIM		2004	Sequencer Instruction Memory 4	4344, page 127	
SIUS SIM		2005	Sequencer Instruction Memory 5	4344, page 127	
SIU6 SIM		2e06	Sequencer Instruction Memory 6	4 3 4 4, page 127	
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SIU9 SIM		2e09	Sequencer Instruction Memory 9	4 3 4 4, page 127	
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SIU11_SIM		2e00	Sequencer Instruction Memory 11	4 3 4 4, page 127	•
SIU12 SIM		2e0c	Sequencer Instruction Memory 12	4344, DBD# 127	
SIU13 SIM		2600	Sequencer Instruction Memory 13	4344 Date 127	
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SIU17 SIM	2011	=	Sequencer Instruction Memory 17	4 3 4 4, 0809 127	
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Table 4-5. VPU Registers Accessed by the Register Data Port (cort)

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CI.-PX2070 Video Processor

Video Processor

C1.-FX2070

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4.3.1 VPU Global Control

4.3.1.1 VPU_MCR: Master Control

I/O Address HIU RDT Index 2000

Register VPU_MCR controls the operation of the IPU1, the IPU2, and the OPU tor helds 1 and 2

ž			¥ 7	0	22.20		IP2f SS	PIFSS
	2	2	2	11	٠	•	7 6 5 4 3	•
911	Access		Reset	Description	<u>د</u>		,	
15.13	P.	_	£	RSVD	Reserv	Reserved (read as 0)	1 as 0)	
12	P.W.			ALUE	ALU Er	Disable Disable Enable	Al U Enable Enables or deables the operation of the ALU Deable ALU operation Enable ALU operation	ALU
	.]	0000	OPFSS	OPU F specific 0000 0001 0011	OPU Field Sync specifies whethy synchronisation 0000 Disable 0010 Start on 0011 Start on 0011 Start on	OPU Field Sync Select. Enables or disables the operation of the OPU specifies whether it processes one or both helds, and specifies the held specifies whether it processes one or both helds, and specifies the held opposition of the action of Start unit on near held, both helds of Start unit on near held, both helds of Start unit on held 1, single held only 0011. Start unit on held 1, took helds of Start unit on held 2, single held only 0100. Start unit on held 2, single held only	man of the OPU
	RVW		0000	IP2FSS	19/12 Fig. 18/12 Fig.	PILO FIELD SYNCHOLOGY SPECTRON OF STATE	Select in the selection of the selection	d specifies the feth
0 0	8	6	0000	PIFSS	PUT FI specifie synchro 0000 0001 0011	iPU1 Field Sync specifies whethy synchronization 0000 Osable 0001 Start un 0011 Start un 0010 Start un	PUT Fleed Sync Select E-habbes or disables he operation of the IPTI specifies whether it processes one or both helds and specifies the horizon at a processes one or both helds and specifies the horizon of the processes one or both helds and specifies are interested to Start unit on held 1 sample held only 5011 Start unit on held 1, sample held only 5010 Start unit on held 2, sample held only 5100 Start unit on held 2, sample held only 5100 Start unit on held 2, sample held only 5100 Start unit on held 2, sample held only 5100 Start unit on held 2, sample held only 5100 Start unit on held 2, sample held only 5100 Start unit on held 2, sample held only 5100 Start unit on held 2.	on of the IMM. Decides the hole

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4.3.2.1 IPU1_PIX: Pixel Count

IN Address HILL HDE

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Register IPU1_FLC returns the current 15 bit field count on read, is set to zero when bit FCE in IPU1_FIR is set to zero.

4.3.2.3 IPUI_FLC: Fleld Count

I/O Address HIU_RDT Index 2102

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Bit & Access Reset Description

RSVD Reserved (read as 0)

Field Count

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Read Only

A Grass Light Company	Video Processor
4.3.2 IPU1: Input Processor Unit 1	=

Register IPU1 PIX is a reart only register that reads back the value of the current 11 bit pixel counter. It automatically resets to 0 at the beginning of each line

PC			Hfnj
RSV0 PC 10 9 0 7 0 9 0 7	Bit g Access Reset Description	RSVD Reserved (read as 0)	100 flead On PC Pirel Count current has (0 7/fh)
	Reset	£	 ! !
15 14 13 17 11	Access	15 11 Read Oh Omb	Read On Only
2	916	15 11	0 01

4.3.2.2 IPUI_LIC: Line Count

M) Address HIU RDT Index 2101

Register IPUJ 1 I IC is a read only register of the current 11 bit line count. It automatically resets to 0 at the beginning of each field

15 14 13 17 11 10 9 0 7 6 5 4 3 2 1 0		d as 0)	100 Read Oi LC I'me Count current feetd (0.71 Fh.) Only	
15 14 17 17 10 9 0	ription	RSVD Reserved (read as 0)	I me Count cu	
=	Bit & Access Reset Description	USVD	2	
nsvo	Ss Res	, &	á	
15 14 13 17 11	Acce	15 11 Read Only	Read Only	-
2	ä	15 1	0 0	

Register IPU1, LIR generates an interrupt request when the 11 bit value in field IRLC is equal to the value in field LC of register IPU1_LLC. VO Address HIU_NDT Index 2103

4.3.2.4 IPU1_LIR: Line Count Interrupt Request

		RSVD 13	3, 12	1 =	2	٥	•	(Al C 1 6 5 4 1 0	•	ا قار د	•	-			_
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										2					
ž	Ξ	2	15 14 13 12 11 10	=	9	, 8 6	•	`			•	0 4 3 7 4 0	~	-	
Bit	Acc	880	Bit # Access Reset Description	Des	criptic	Ę								:	:
15 11	15 11 RVW		£	RSV	0	RSVD Reserved (read as 0)	d (read	1 as 0)							
100	P/W		ક	₹		IRt C Interrupt Request Line Count (0.71 Fts)	Peg.	12.	3	9	Ξ	mupi Request time Count (0.7FFh)	:		

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4.3.2.5 IPU1 FIR: Flekt Count Interrupt Request

I/O Andress HILL HILL HILL Index

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P generales an interrupt request whe	eto IDI I II C
IP generales an interrupt request whe	Meter IDITI CI C
FIR generates an interrupt request when the 15 bit value in field IDEC is assisted to	Carlos IDI 11 Carlo
FIR generates an interrupt request whe	Policios IDELL C. C.
1 FIR generates an interrupt request whe	Constant Dill City
U1 FIR generates an interrupt request whe	of register 10111 City
101 FIR generates an interrupt request whe	of recietae 10t11 Ct C
PU1 FIR generates an interrupt request whe	Of tooleto, 10111 Ct
IPU1 FIR generates an interrupt request whe	C. of register 19111 Ct.
er IPU1 FIR generales an interrupt request whe	FC of register 1911 Ct.
ler IPU1 FIR generates an interrupt request whe	d FC of conjeto, 19111 Ct
ister IPU1 FIR generates an interrupt request whe	MARC of register 1911 C. C.
egister IPU1. FIR generates an interrupt request whe	the telephone in the contract of the contract

DHIC INIC	0 1 2 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0	Bit # Access Resel Description	Field	t held count enabled O held count disabled	IRFC Interrupt Request Field Count
	0 1 2 1 10	Oescrip	1CE		IRC
		Reset	£		£
		Access	75		₹
ğ :		911	5		14 0 FVW

4.3.2.6 IPU1_LRB: LUTRAM Base Address

HILL RDT I/O Address Register IPU1. LRB preloads the 8 bit LUT RAM address counter and initiatizes the channel pointer to the YR channel. The channel pointer automatically advances to the next channel alter each LUT RAM access. And address counter automatically increments after accessing the Cr8 channel. LUT RAM elements are accessed in the following order. YRLRB+01, Cr8[RB+0]. Cr8[RB+0]. YRLRB+1]. CbG[LRB+1].

VII	7 6 5 4 3 2 1 0	
RSVO	15 14 13 17 11 10 9 6 7 6	Bit A Access Acc

Access Reset Description

NSVI) Reserved (read as 0)	70 PVW On LINI LUI RAM Rase Address Specifies the Bibit address	value (OTTh)
USAD	2	
ŧ	£	Î
P.W	5	
15.8	0,	

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4.3.2.7 IPU1_LRD: LUT RAM Data

I/O Address HIU RDT

IPU1_LRB_LUT RAM Base Address, p. 108

See also

Register iPU1, LRD is the bidirectional data port to the storage elements of the three channel LUT RAM

1				s to the current LUI
. tAD	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		(0	LUT FAM Data Data writen to this held transfers to the current LUT RAM element, gata to be read from the current LUT TAM element appears in this field (0 FFh)
	_		RSVD Reserved (read as 0)	of data D.
	Ŀ		\$	7 9 E
	۰	5	Peser	UT II
	ō	cripti	و و	
6	=	ĕ	лSv	LAD
RSVD	15	Rosel	8	ક
		Access	P/W	Rvw
	15	Bil # Access Resel Description	15.8	. 02

4.3.2.8 IPU1_MCRI: Mester Control

I/O Address Index

HUU RDT 3000 (IPU1_MCR1 Master Control Field 1) 3100 (IPU1_MCR2 Master Control Field 2)

Special Y Scaling Path Mode, p. 57 IPUI, Impul Processor Unit 1, Section 3.3.2 on page 50 Figure 3.16 IPUI impul Processor Unit 1, p. 51

Registers IPU1_MCR1 and IPU1_MCR2 control the operation of the IPU1 for fields 1 and 2

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		6 8 4 5
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	ASA	9
	IE	=
	CSCE	2
	PSE	2
	3	2
Ī	FPS	5
•		

911	Access	Reset	Bit & Access Reset Description
ā.	P.W	•	FPS Field Potanty Select Controls the potanty of the India II) signal surplined to the Window Capping and XY Scaler O Normal potanty I Invest potanty
:	P.W	0	IM Interface Mode Specifies the input steam as interfaced or non untividuced data 0. Progressive scan input

Interfaced input

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Bit & Access Reset Description (ront)

	Prescaler I native Enables or disables the operation of the X Prescaler O Opposa prescaler (X prescaler Enable 0.5 X prescaler	Color Space Converter Enables or disables the operation of the Color Space Connecter of Pipass color space converter of Pipass color space converter or Enable color space converter.	1UT Enable Enables or disables the operation of the LUT RAM 0 Oppass LUT RAM 1 Enable LUT RAM	Y Scaling Path Enables or disables the special Y Scaling Path Mode. Y Scales performs Y scaling At Uperforms Y scaling	Outbut Data Tag Controls the input selection of the Input Tag Unit tag multiplesor (see Figure 3.27) 00 Fass Tag unchanged 01 Set tag to inverse chroma key Tag 11 Set tag to be format key Tag 11 Set tag to chroma key Tag	15	¦6
00000		i	: :: ::	YSP		! ! !	
	0		:	!	8	0000	0000
	*4	P.W.	W.	3. *	M ₂		

4.3.2.9 IPU1_XBnf: X Begin

HIU, NDT 3002 (PUL), XBF1 X Begin Fraction Field 1) 3002 (PUL), XBF2 X Begin Integer Field 1) 3101 (PUL), XBF2 X Begin Fraction Field 2) 3102 (PUL), XBE2 X End Integer Field 2) I/O Address Index

Section 3.3.2 on page 50 Section 3.3.2.5 on page 56

Registers IPU1_XBnf specify the 11.3 format X begin value for fields 1 and 2.

See also:

IPU1, XBF1 and IPU1, XBF2 allow the virtual left boundary of the post scaled window to be aligned bri tween pixels of the pre-scaled window for fields 1 and 2. X Begin Fraction Indea (IPU1_XBF1 and IPU1_XBF2)

	*								ASVO						RSVO
5	2	2	2	=	9	۰	-	_	•	5	6 5 4 3	-			<u>:</u> •
						i]		i	: .	<u>:</u>	<u>:</u>

Access Reset Description

15 13	15 13 RW	£	96	Begin X Column Fractional Index. Specifies the 3-bit fractional portion
				of the 11 3 formal X begin value (0 7h) .
120	12.0 PVW	£	RSVO	RSVD Reserved (read as 0)

X Begin Integer Index (IPU)_XBI1 and IPU1_XBI2)
Registers IPU1_XBI1 and IPU1_XBI2 define the left boundary of the pre-scaling window for helds 1 arr
2. Alf video to the left of this boundary is clipped and is not used to generate the scaled window

		ASVO							 	6			:		1
š	•	13	21	=	5	•	•	-	•	5	1 2 4 3 3	'n	.~	_	٠.
100	¥c	888	Access Reset Description	å	criptio	e				i :		į		:	:

Begin X Column hiteger Index Specifies (the 11 bit integer pontish of the 11 3 format X begin value (0.711 h) RSVD Reserved (read as 0) æ ٤ £ **₹** P.W 15 11 00

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4.3.2.10 IPUI_XEII: X End

100 081 MO Address

3003 (IPIJ) XEII X Enclineger Field 1) 3103 (IPIJ) XEI2 X Enclineger Field 2)

Figure 3.18 Window Clapping and XY Scaling Control Registers, p. 56

See also

Registers IPU1 XE11 and IPU1 XE12 specify the 11 bit X end value for fields 1 and 2.

Bit# Access Reset Description

RSVO Reserved (read as 0)		X Ford Cohuma Integrate Towns Consults A.	THE COMMITTEE OF THE PROPERTY OF THE PARTY AND THE PARTY OF THE PARTY
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15 11 P.W	!	10 0 IVW	

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I/O Address frdex

4.3.2.11 IPU1_XSnf: X Shrink

HIU, RDT 3005 (PUI, XST1 X Shunk Fraction Field 1) 3005 (PUI, XSI1: X Shrunk Fraction Field 1) 3104 (PUI, XSI2: X Shrunk Fraction Field 2) 3105 (PUI, XSI2: X Shrink Integer Field 2)

Figure 3-18 Window Cipping and XY Scaling Control Registers, p. 56 See also

Registers IPU1_XSnl specify the 6.10 formal X shrink value for fields 1 and 2.

X Shrink Fraction (IPU1_XSF1 and IPU1_XSF2)

!	0
RSWD	6 5 4 3 2 1 0
RSVD	~
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Bit & Access Reset Description

- '	15.5	15.5 RVW	,	8	75	7 =	Sheina Nak X si	h Fraci	X Shrink Fraction. Specifies the 10-bit fractional portion of the 6-10 for that X shrink value (0.3Fh)	Of Fh	₽ _	<u> </u>	ctional	portio	8	ê 6 10	ğ
▼ 1	اء	ě	RvW Oh	£	RSVD Reserved (read as 0)	•	lesere	rd (rea	d as 0)		ĺ				!	:	į
	Shrie	at Tieg	(<u>a</u>)	UI_XSI	X Shrink integer (IPU1_XS)1 and IPU1_XS)2)	×,	(Z)							! -	į	i.	ļ.
_					RSVD						_	:	15	. 2	:	:	:
	ž	:	13	12	15 14 13 12 11 10 9 8 7 6 5 4 1 2 1	٥	-		_		-	_			_	_	٠,

Access Reset Description

RSVD Reserved (read as 0)

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X Shrink brieger Specifies the 4 bi integer portion of the 4-10 formal X shrink value (0 Fn)

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4.3.2.12 IPU1_YBnf: Y Begin M) Address Index

HIU RDT 3006 (PVI YBF I Y Hequi) 3006 (PVI YBF Y Hequi) 3106 (PVI YBF Y Hequi) 3107 (PVI YBF Y Hequi)

Figure 3.18 Window Cipping and XY Scaling Control Registers, p. 56

Registers IPU1_YBnl specify the 11.3 format Y begin value for fields 1 and 2.

Y Begin Fraction Index (IPU1_YBF1 and IPU1_YBF2)

Registers IPU1 VBF1 and IPU1 VBF2 allow the virtual top row of the post scaled window to be aligned between rows of the pre-scaled window for fields 1 and 2

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Bit # Access Reset Description

Regin Y flow Fractional Index. Specifies the 3 bit fractional portion of	the 11 3 formal Y begin value (0.7h)		12.0 RVW Oh RSVD- Reserved (read as 0)
96	Ě		RSVD- R
£			f
15 13 RVW			₽ .
15 13		!	120

Y Begin Integer Index (IPU1, YB11 and IPU1, YB12)

Physicies IPUT YBIT and IPUT YBI2 define the top edge of the pre-scaling window for fields I and 2. All video above this boundary is clipped and does not become part of the scaled window.

Ha Ha	Bit # Access Reset Description	Reset	Descrip	llon
15 11	15 11 PVW	8	nsvb	NSVD Reserved (read as 0)
0 0	FVW	£	. .	10.0 IVW On BI Begin Y Row Integer Index Specilies the 11 bit integer portion of the 11 J formal Y Degin value (0.71f h).

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CL.PX2070 Video Processor

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4.3.2.13 IPU1_YEII: Y End

HBU_RDT NO Address Inder

3006 (IPU) YEIL Y End Integer field 1) 3108 (IPU) YEIL Y End Integer Field 2)

Registers IPU1_YE11 and IPU1_YE12 specify the 11 bit Y and value for helds 1 and 2 Figure 3:18 Window Clipping and XY Scaling Control Registers, p. 56 See also

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	ASVO		=		
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Access	

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15 11 RVW On RSVD Reserved (read as 0) 10 RVW On E1 End Y flow integer int	6	End Y flow Integer Index Specifies the 11 bit Y end value (0.71 Fh)	
On RSVD Reserved On Et EndYRo	ead as (Integer	
On RSVD	Reserved (r	End Y Row	
15 11 FVW Oh 10 0 FVW Oh	RSVD	Œ	
15 11 FVW 10 0 FVW	٤	£	
100	8	*	
	15 11	9	2

4.3.2.14 IPUT VSnf. Y Shrink

100 001 IN) Arthess

3009 (IPT) VSF1 V Shunk Fraction Field 1) 3008 (IPT) VSF1 V Shunk Integer Field 1) 3109 (IPT) VSF2 V Shunk Fraction Field 2) 3108 (IPU) VSF2 V Shunk Integer Field 2)

Figure 3.18 Window Clipping and XY Scaling Control Registers, p. 56

Registers IPU1, YSnt specily the 4 10 format Y shrink value for fields 1 and 2.

Y Shrink Fraction (IPU1_YSF1 and IPU1_YSF2)

Access Reset Description

Y Shrink Fraction Specifies the 10 bit fractional portion of the 4-10 formal Y shrink value (0.3FFh) š £

NSVI) Reserved (read as 0)

Y Shrink Integer (IPU1_YSI1 and IPU1_YSI2)

Access Resel Description

Y Shurth Integer Specifies the 4-bit integer portion of the 4-10 format Y RSVD Reserved (read as 0) Shrinki value (0 f.h) ٤ ٤ **₹** 3

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HIU, ROT I/O Address

4.3.2.15 IPU1_KFCI: Key Function Code

3005 (IPU1, KFC1 Key Function Code Field 1) 310b (IPU1_KFC2 Key Function Code Field 2)

Registers IPU1_KFC1 and IPU1_KFC2 specify eight 1 bit values used by the key function code multiples Figure 3-17 Input Tag Unit, p. 55 See also

ers for fields 1 and 2.

KEYEC Key Function Code Species egit I bi input values used by the key function code multiplexers (0 F h) 12 11 10 9 0 7 6 5 4 3 2 1 0 RSVD Reserved (read as 0) Access Reset Description £ 동 Ž ş

4.3.2.16 IPU1_MMxf: Chroma Key Max/Min

HIU ROT I/O Address

300C (IPU1 MMAY1, Chroma Key VRR Mau/Min Field 1)
300C (IPU1, MMAY1, Chroma Key UG Mau/Min Field 1)
310C (IPU1, MMAY2, Chroma Key VRR Mau/Min Field 1)
310C (IPU1, MMAY2, Chroma Key VRR Mau/Min Field 2)
310C (IPU1, MMAY2, Chroma Key UG Mau/Min Field 2)
310C (IPU1, MMAY2, Chroma Key UG Mau/Min Field 2)

Registers IPU1, MMMI specify the maximum and minimum 8 bit chroma key comparator values usnd by the Input Tag Unit for fields 1 and 2. These values are used for each of three 8 bit input channels for both fields 1 and 2 (see Figure 3.27).

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4.3.3 IPU2: Input Processing Unit 2 4.3.3.1 IPUZ PIX: Pixel Count

I/O Address HIU RDT Index 2300



Key Y/R Maximum/Minimum (IPU1, MMY1 and IPU1 MMY2)

:	1						YHMIN	Z			
	2	-2	<u> </u>	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		-	·	c	2	-	٥
911.0	Bit # Access Reset Description	Reset	Descrip	Hon							
158	15.8 RVW	£	YIIMAX	YIIMAX Key YAT Maximum Specifies the upper threshold for the 8 bit Y (YCbC) stream) or R (RGS stream) channel comparator (0.FFh)	tum Specif TGB stream	es the up	Ser three	ator (6	1 E 1	<u>ک</u> کو خ	ğ
7.0 FVW	N.W.	6	YIMIY	YRMIN Key Y/R Minmum. Specifies the lower lineshold for the 8-bit Y (YCbCr stream) or R (RG8 stream) channel comparator (0-FTh)	um. Specifi IGB stream	es the low	or thres	bo of	1 E	<u>ک</u> ۸	ğ

Register IPU2, PIX is a read-only register of the current 11 bit pirc) count. It automatically resets to 0 are the beginning of each line.

RSVD

Pixel Count current line (0.7FFh)

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4.3.3.2 IPUZ_LIC: Line Count

MO Address HIU_RDT Index 2301

RSVD Reserved (read as 0)

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Pread Only 9 g 1

15:11

Access Reset Description

Key UrG Meshrum/Minhnum (IPU1_MMU1 and IPU1_MMU2)

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į	TYWWY)	5	CHIMAK						ğ	COMEN			
2	15 14 13 17 11 10	2	=	2	٥	•	-	[s]	-	-	~		°
18	Access Resel Description	Resel	es O	criptic	Ę								
15.8	P.W	æ	2		3		MAN WALLES						

UCMAX Key UG Marimum Specifies the upper threshold for the 8 bit Cb (YCb-C) Stream or G (RCR) stream in hander concessors to Exist.	70 FVW On UGMIN Key LVG Minmum Specifies the lower liveshold for the 8 bit Cb (YCb.	Cr stream) or G (IIGB stream) channel comparator (0.FFh)
NON	UGMII	
£	PAW 95	
ISA RW	F.	
15.8	0/	

Register IPU2_LIC is a read only register of the current 11 bit line count. It automatically resets to 0 at the beginning of each field.

Line Count current field (0 7Ff h)

RSVO Reserved (read as 0)

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Read Only Read Only

11.11

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Bit # Access Reset Description

ASVD

Key V/B Maximum/Minimum (IPU1_MMV1 and IPU1_MMV2)

İ						ARMIN	_		
2	[18 14 13	2	e =	15 14 13 12 11 10 9 6 7 6 5 4 3 2 1 0	9 /	•	2		0
100	Access	Reset	Bit # Access Reset Description	lion					
8.8	15.8 RvW	5	VBMAX	VBMAX Key V/B Maxmum Specifies the upper threshold for the 8 bit Cr (YCb-Cr stream) or 8 (RGB stream) channel comparator (0-FFh)	Key V/8 Maximum. Specifies the upper threshold for the 8 bit Cr stream) or 8 (RGB stream) channel comparator. (0.FFh)	e upper thresho	ator (0.FF	O E	Įĝ
		£	VBMIN	VBMIN Key V/8 Minmum Specifies the lower threshold for the 8 bit Cr (YCBC) stream) or 8 (RG8 stream) channel comparation (16 FF);	Key V/B Minimum. Specifies the lower Ihreshold for the B. stream) or B. (AGB stream) channel comparator. (0.FFh)	lower threshold	d for the 6	DAI CO (YC	မွ

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4.3.3.3 IPUZ FLC: Field Count

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Address	

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Address	

15 bit field count.
Creturns the current
FIC
y IPU2
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On read

HSV0	RSVD					5					
٠	01 11 21 61 10		٦				•	•	~		
ā	Access Reset Description	Roset	Descri	ption						ļ	
5	Read Only	£	USAD	NSVD Reserved (read as 0)	red (read	8					
	nead Only	8	FC Freid cour	Field count	5						

4.3.3.4 IPU2_LIR: Line Count Interrupt Request

I/O Address HIU ND1 Index 2303

Register IPU2, LIR specifies an 11 bit line count value that generales an interrupt request when equal to the realtime line count value in register IPU2_LIC.

115 FAW ON RSVD Reserved (read as 0)

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4.3.3.5 IPU2_FIR: Field Count Interrupt Request

I/O Address HIU_RDT Index 2304

Register IPU2_FIR specifies a 16-bit field count value that generates an interrupt request when equal to the realtime field count value in register IPU2_FLC.

ñ z

81t ¢	Access	Bit # Access Reset Description	Descrip	lon
5	ΡW	•	FCE	
140	RVW	8	IRFC	Interrupt Request Freld Count
4.3.3.6	IPU2 M	4.3.3.6 IPU2_MCRI: Mester Control	ter Contr	
I/O Address Index		HIU ROT 3200 (IPU2, M 3300 (IPU2, M	CRI. Mass CR2: Mass	HIU RDT 3200 (IPU2, MCR1, Master Control Field 1) 3300 (IPU2, MCR2 - Master Control Field 2)
See also		ure 3-19 tr ure 3-21. IF	Put Proces	Figure 3:19 Input Processing Unit 2; p. 60 Figure 3:21: IPUZ Window Chiping Unit, p. 62

Registers IPU2_MCR1 and IPU2_MCR2 control the operation of the IPU2

FPS	3	PSE								=	ASVD								
2	2	2	2	=	9	•	Н			H	•			- 1		•	~	\mathbf{H}	
2	¥C		Access Reset Description	å	夏	5	- 1	I		į				1			- [
5	P.		8	§.		Field Potanty Select. Controls the potanty of the field ID signal supplies to the XV Window Clipping subunit. Normal potanty Invert potanty	8 × 2 E	A A E	Marry Select (Y Window Cir. Normal polarity Invert polarity	Ranty Select Co Y Window Clipp Normal polanty Invert polanty	20 00	S P	<u> </u>	, A	Ě	į	Ē,	5 :	,
2	A.		ક	3		mentace Mode Specifies the input stream as interlaced or non-interaced data Progressive scan input Hitterlaced input	2 2 2 2	0 0 E	3	Mode Specifies the site Ha Progressive scan input Interfaced input	12 Z	2	2	i e a	whyd stream as w	, i	ž.	8	§ .
C.	P.W.		£	PSE		Prescaler Enable Enables or distribes the operation of the K Prescaler Pypass prescaler Finable 0.5 K prescaler	ا يَبْ هُمْ ا	E S S	200	er Enable Enables or di Bypass prescaler Enable 0 S X prescaler	es o	: 3 0 2	. Sec	i g	or disables the operation of the	E C	, <u>E</u>	¥ .	. 5
120	FVW		£	RSVD	1	Reserved (read as 0)	8	1		i	:		:						

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RSVD Reserved (read as 0)

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4.3.3.7 IPU2_XBIT: X Begin

IV) Andress HIU RI)1 Indet 3202 (IPU2 XBI X Brgin Integer Field 1) 3302 (IPU2 XBI2 X Begin Integer Field 2)

Figure 3.21 IPU2 Window Clipping Unit, p. 62 See also

Registers IPU2_XBI1 and IPU2_XBI2 specify the 11 bit X begin value for lields 1 and 2.

_			
		0	
		$\lceil \cdot \rceil$	
-	ā		
-			
-		2	
1		=	
!		2	
	ASVD	5 14 13 17 11 10 9 0 7 6 5	
!		=	
!	_	2	

Access Reset Description Bit

1511	¥.	5	RSVO	15 11 IVW Oh RSVO Reserved (read as 0)
0 01	10 WW Oh	11 fVW Oh BI BeginXC	ē	Degin X Column Integer Index Specifies the 11 bit Integer portion of the 11 0 format X begin value (0.7F h)

4.3.3.8 IPUZ XEII: X End

HIU RD1 3203 (IFU2 XFH X End Integer Field I) 3303 (IFU2 XEL2 X End Integer Field 2) I/O Address

Figure 3.21. IPU2 Window Cipping Unit, p. 62 See also

Registers IPU2 XE11 and IPU2, XE12 specify the 11 bit X end value for helds 1 and 2.

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		[-]
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i		-
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:		٥
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		=
į		[=]
1	RSVO	2
		2 6 5 6 5 6 5 6 5
1		[2]

Access Reset Description 100

		idex Specifies the 11 bit X endivative (0.7FFh)	
Reserved (read as 0)		tind X Column Integer Inde	
ASVD		=	
8	-	5	
3		X	
15 11		002	

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4.3.3.9 IPU2_YBII: Y Begin

3207 (IFU2_VBI Y Bagin Integer Field 1) 3307 (IFU2_YBI2. Y Bagin Integer Field 2) Figure 3-21. IFU2 Window Cipping Umi. p. 62 I/O Address HIU_RDT

See also.

Registers IPU2_YBI1 and IPU2_YBI2 specify the 11 bit Y begin value for fields 1 and 2	. 16
Registers IPU2_YBI1 and IPU2	ASVD

ū

Access Reset Description

_,	12	RW	8	RSVD	Reserved (read as 0)
_	00	¥ ¥	5	5	Begin Y How integer index Specifies the 11 tot integer portion of the
					11 bit Y begin value (0 7FFh)

4.3.3.10 IPU2_YEH: Y End

I/O Address

HIU_RDT 3208 (IPU2_VEI) · V End Integer Freid 1) 3306 (IPU2_YEI2 · V End Integer Freid 2)

Figure 3:21 IPU2 Window Cipping Unit, p. 62 See also

Registers IPU2_YEI1 and IPU2_YEt2 specify the 11-bit Y end value for fields 1 and 2

:	
	- ;
:	1 2 5 1 4 1 3 5 5 6
	_
ū	
	•
	_
	•
	9
	=
	[2]
RSVD	[2]
	2
	2

Access Reset Description

RSVD Reserved (read as 0)	End Y Row Integer Index Specifies the 11 bit Y end value (0.71 fri)	
RSVO		
ક	٤	
FVW	P	
15 11 RVW	100	

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4.3.4 StU: Sequencer Instruction Unit

4.3.4.1 SIU MCR: Mester Control

In Andress HIU RDF Index 2800

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13 35 0xsu	2
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nsvo se	
_	_

Bit & Access Reset Description

15 14		£	ASVD	Reserved (read as 0)
2) ()	'	R.W 00	35	Sequencer Enable. Enables or disables the operation of the SIU 00 SIU halted SI enabled, start on SI 1 SIU enabled, start on SI 2
0	P.W.	8	-	Freid Toggle Specifies the field toggle mode and the association of the start index values to a head. On No field toggle (SI is used, SI? is sprored) O1 SI and SI2 toggle on ventical syre, no field association Freid 1 is associated to SI1, and fields 1 and 2 toggle on vertical syre.
9.8	¥	£	25	Start Index 2 Specifies the 5 bit sequencer instruction start index 2 (0. 1f.t)
0	40 FVW On SII	8	Sir	IVW On Sit Stanlinder 1 Specifies the 5 bit sequencer instruction stant index 1, (0-14 h)

4.3.4.2 SIU_FCS: FIFO Control Status

1:O Address HIU, HDT Index 2801

Register StU_FCS is a special readwrite register that provides realtime access to the full and empty flags from FIFOs A G_AB flags are active high. Writing a 1 to FIFO Empty Flag helds resets the corresponding FIFOs_Writing a 0 to FIFO Empty Flag lields enables the corresponding FIFOs.

	_	_	_	
	3		•	,
	TAS TAS		-	
	FRE		,	
	rB.r		-	
	F.C.	i	-	-i
۱ ا	T 10E FCF FCF FBF	İ	٠.	-
	30.	i	٠	-
İ	ě	i	_	-
Ì	<u>.</u>	<u>+</u>	-	
<u>.</u>	=	:	<u>-</u>	-
-	=	· :	<u> </u>	-
	101 201 101 111 111 101		<u> </u>	
ŀ	<u>-</u>		-	
+	<u>.</u>	<u> </u>	_	j
-	_	1	- -	
1	340	<u>:</u>	<u>-</u>	-
- ; '	_	•	•	

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Description	
Access Reset	
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0						- 0.5								
Reserved (read as 0)	FIFO G Full Flag	FIFO G Empty Flag On read empty flag On write, FIFO reset	FIFOF Full Flag	FIFO F Empty Flag On read empty flag On write: FIFO reset	FIFO E Full Flag	FIFO E Empty Flag On read empty flag On write FIFO reset	FIFO D Full Flag	FIFO D Empty Flag On read empty flag On write FiFO reset	FIFO C Full Flag	FIFO C Empty Flag On read empty flag On write FIFO reset	FIFO B Futt Flag	FIFO B Empty Flag On read: empty flag On write FIFO reset	FIFO A Full Flag	FIFO A Empty Flag On read empty flag On write FIFO reset
RSVO	rGF	20.	666	37.	125	FEE	FOF	FDE	FCF	25.	7.B.F	£ 9E	FAF	FAE
ક	£	£	ŧ	£	£	8	£	ક	£	ક	£	£	8	£
RW	Rd only	8	Rd only	P/W	Ad-only	P.W	Rd-onty	RVW	Rd only	FA.W	Ad only	A.	Pd onty	æ.
15 14	£1	21	=	0	6		7	9	S		c	~	_	۰

CL-FX2070 Video Processor

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4.3.4 SIU: Sequencer Instruction Unit 4.3.4.1 SIU_MCR: Mester Control

LO Aridress HIU RUT Index 2800

Register SIU, MCR controls the operation of the SIU for fields 1 and 2.

115VD SE	0 6 01	115VD SE F1	HSVD 15 14
----------	--------	-------------	---------------

Bit# Access Reset Description

15 14	N.	£	RSVD	-
21 (1)	3	7vw 00	SE	Sequencer Enable Enables or disables the operation of the StU. 00 StU halted 10 StU enabled, start on St1 11 StU enabled, start on St2
0	M.	00		Fired Toggle Specifies the field toggle mode and the association of the start index values to a held toggle (Stirs sproted) to No held toggle (Stirs used, SCR is sproted) to Stirand Stiroggle on vertical syric, no field association field is associated to Stir, and helds 1 and 2 toggle on vertical sync sync syric strains to start field is associated to Stir, and fields 1 and 2 toggle on vertical sync
s 6	3	95 IVW On SI2		Start index 2. Specifies the 5 bit sequencer instruction start index 2. (0. 1f h)
0	¥.	40 RW Oh	SE	Start Infex 1. Specifies the 5-bit sequencer instruction start index 1. (0. 1f.n)

4.3.4.2 SIU_FCS: FIFO Control/Status

LO Adgress HILL RDT Index 2801

Register StU_FCS is a special read/write register that provides realitine access to the full and empty flags from Fif Us A_G_All flags are active high. Writing a 1 to FiFO Empty Flag fields resets the corresponding Fit Us. Writing a 0 to FiFO Empty Flag fields enables the corresponding FIFOs.

38	1	`	
FEE FOF FOF FCE FBF FBE		_	
FCE	i	•	
101		~	
ē	:	۰	
٥	!	~	
FEE		•	-
Ξ		0	•
11.6		9	
Ξ		=	į
7.0E		~	
õ		=	. 1
SVO FGF FGE FFF FFF		•	!
H5V0	_	<u>.</u>	:

FAF FAE

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Bit# Access Reset Description

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4.3.4.3 SIU_FOU: FIFO Overflow/Underflow

I/O Arkhess HIU, HDT Index 2802

Prejister SRI FOU is a rinad only register that provides realtime access to the overflow and underflow flags from EIFOS A G. All flags are active high (overflow, underflow = 1).

_	
FAU	•
FAO	-
36	2
8	-
3	-
032	\$
3	•
8	-
13	
9	•
E	2
101	=
1 <u>0</u>	2
nsvn rao rau rro rru rro reu roo roo rao rao rau rao rau	5 14 13 17 11 10 9 6 7 6 5 6
: : :	2
USVD	_

Access Reset Description 911.6

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CL.-PX2070 Video Processor

CL.-PX2070 Video Processor



4,3.4.4 SIUs_SIM: Sequencer Instruction Memory

O Address	HIU_RDT			
ndex	2e00 (SRJO_SIM)	2e08 (SIUB, SIM)	2010 (SR116, SIM)	2e18 (SR124 SIM)
	2601 (SIU1_SIM)	2e09 (SIU9, SIM)	Zeri (SRJ17 SIM)	2e19 (SR125_SIM)
	2e02 (SRJ2 SIM)	2e0a (SIU10 SIM)	2012 (SRJIB SIM)	2018 (SRI26 SIM)
	2e03 (SIU3 SIM)	2e0b (SIU11, SIM)	Zein (SIU19 SIM)	2e15 (SI127 SIM)
	2e04 (SRJ4_SIM)	2e0c (SIU12, SIM)	2e14 (SIU20 SIM)	201C (SILIZB SIM)
	2e05 (SIUS SIM)	2e0d (SIU13 SIM)	2015 (SR121 SIM)	201d (SRI29 SIM)
	2e06 (SRU6_SIM)	260e (SIU14 SIM)	2e16 (SIU22 SIM)	Zele (SRI30 SIM)
	2e07 (SRU7 SIM)	2edf (SIU15 SIM)	2417 (SIL)23 SIM)	2ett (SIU3) SIM)

The 32 identical registers SIUs_SIM store the instruction sequence for helds 1 and 2

	HSVD	Ş			OTN		43	FA	VB5
	ıs	•	C.	12	11	,	•	, 6 5 4	3 2 1 0
	ii ii	Acc	Access	Resot	Description	ofton			
	15 14	Ş		£	PSVD	Reserv	Reserved (read as 0)	(0 se	
	139	¥.		£	NIO	Offset 1 the nex	o Next	Offset to Next Instruction. Specifies the signer of the next instruction to execute (0.1fh)	l displacement
_		PVW	,		a.	Ent Po held to	Normal Fat po	Est Pord identifies the current instruction as the est point when the field loggle condition is delected. Normal fall through instruction. Est point instruction.	on as the eart point when the
-	*	P.W.		0000	.	0000 0001 0010 0011 0110	SSOCIATION FIFO FIFO BRIED BRI	n Associates a F IF O with	The Current instruction
_	30	FO.		0000	8 ₩	Object 0000 0000 0001 0001 0001 0001 0001 00	Buffer Association (see held f./ Object bufer 1 Object bufer 2 Object buffer 2 Object buffer 3 Object buffer 3 Object buffer 5 Object buffer 5 Object buffer 5	on Associat	hect buller with the Current

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438 ALU: Arithmetic and Logic Unit

4.3 5.1 ALU_MCRI: Master Control

I/O Address HILL HILL 2900 (A11) MCH1 Master Control Field 1) 2901 (A11) MCH2 Master Control Field 2)

ALU Anthmetic and Logic Unit, p. 63 See also

Registers ALU, MCR1 and ALU_MCR2 specify the ALU operating mode for fields 1 and 2.

,		_	_	
	OPAS	-	•	
	OPBS		-	
	S		~	
	5	Ľ	_	
Ĺ	3	Į.	•	
	5	ŀ	n	
	3	•	•	
	5	ŀ	•	
	?			
		•		
٩	i	2		
dQV		=	1	
	!	~	1	
JBW IF		2	1	
j =	i	-	j	
Ä	<u> </u>	_	i	

1	Access	Reset	Access Reset Description	cription
	₩ *	8	CHM	Three-operand B4 Mash selecting tag source 64 per bin mask — one 16 bit value in FIFO C will mask one pix- et in the A11, tag bit per bit) 94 per per eff mask — one 16 bit value in FIFO C will mask 16 pixels in the A11, from tan be one 16 bit value in FIFO C will mask 16
	9.7E	0000	;	1ag For
	**		400 V	Authmeticonomic of the control of th
	PW 0	8	YOUT	Y output Source Select

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CL.-PX2070

Bit# Access Reset Description

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		pister	gester
V output Source Select 00 Source output from togical unit 11 Source output based on control tag 11 Enable arithmetic out based on tag	Operand C Source Select O Operand sourced from constant register O Operand sourced from Fit O	Operand B Source Select 0 Operand sourced from constant register 1 Operand sourced from Fiff O	Operand A Source Selecti 0 Operand Sourced from constant register 1 Operand sourced from FITO
V 001	OPCS	OPBS	OPAS
•	0	0	0
8	RW	RvW	FVW
	~	-	0

4.3.5.2 ALU_TOP: Tag Operation

VO Address HIU RDT Index 2902

Data Tagging, p 66 See also.

Register ALU_TOP specifies the control and output tag multiplexer operation codes

:	_
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:	,~;
: . ن	•
: 5	
	\$
010	7 6 5 4 3 7
	7.1
	-
	9
	=
25	
	=
	2
_	نــــــــــــــــــــــــــــــــــــــ

	Access Reset Description	· .	Access Reset Description		criptle	٠ ۾	•		•	^	-]	~ :	'
15.8	8		٤	٤		1 2			;	Ì			l	
0,2	PW		5 8	200		Output Tag Code (0 FFn)) e (0 F	1			į	:	

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Source output from logical unit
Source output from antimietic unit
Source output based on control lag
Enable antimietic out based on lag

852=

Source output from logical unit
Source output from arithmetic unit
Source output based on control tag
Enable arithmetic out based on tag

U output Source Select
00 Source output from
10 Source output from
10 Source output has

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43.5.3 ALU AV: Alphe Velue

1111 RD1 2903 MO Arkiness

Anthmetic Operations p 67 See also

Table 3.23 Arithmetic Operations, p. 67.

Register ALLE AV specifies the alpha mix constant

	۰
	7
	•
	•
	0
•	=
ž	15 14 13 12 11 10 9 0
	2
	=
	51

15 14 13 17 11 10 9 8 7 6 6 1 1 6 1 9 1 1 1 1 1 1 1 1 1 1 1 1 1	8 7 6	•		6		
---	-------	---	--	---	--	--

4.3.5.4 ALU_LOPx: Logic Operation

TOP UNI NO Address Index

2904 (ATU LOPY Logic Operation Channel Y) 2905 (ATU LOPU Logic Operation Channel IJ) 2906 (ALU LOPV Logic Operation Channel V)

Logical Operations, p. 67 See also

Registers ALU LOPY, ALU LOPU, and ALU LOPV specify the constant values for logical multiplexers A, B, and C, respectively.

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	15 14 13 17 11 10 9 0 7 6 5 4 3
	15

Access Reset Description

Mt OP Multiplexor Logical Operation ٤ Š

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#"H 6"'H 6"'H 6"'H 16"; 11.11. ""H

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4.3.5.5 ALU_CAK: Constant A

HIU, RD VO Address

2907 (ALU CAY Constant A. Channel Y) 2908 (ALU CAU Constant A. Channel U) 2909 (ALU CAV. Constant A. Channel V)

ALU_MCRI Master Control, p. 128 See also Registers ALU CAY, ALU CAU, and ALU CAV specify the constant values for Operand A, based on the value of field OPAS in register ALU MCRI.

			USVD							İ	٥	NOD	:	;	:	
5	=	2	15 14 13 12 11 10 9 0 7 6 5 4 3 2 1		2	٠	•	`	٠	s	•	7 6 5 4 3 2	~	-		٠,
911.0	Acc	88	Bit # Access Reset Description	å	scripti	5										
15.9	RvW		£	RS	۶	RSVD Reserved (read as 0)	d (read	(0 se								
	\$		£	146		Tag Specifies the constant tag but to msert in the input stream (0 11)	ecrlies t	the con	Stant la	30 tei 10	n msen	o insert in the input stream (0.1h)	200	ream	9	: =
0,0	¥		£	8		Constant Specifies the constant 8 bit value to use in place of the real time imput stream channel for operand A (0 11 n)	# Spec	Hes H	es the const	ani 8 b	1 4 5 4 5 4 5 4 5 4 5 4 5 4 5 4 5 4 5 4	bit value to use in place of the real	e C	0	. e	i 74

4.3.5.6 ALU_CBx: Constant B

HIU, RDT VO Address Index

290a (ALU CBV Constant B Channel Y) 290b (ALU CBU Constant B Channel U) 290c (ALU CBV Constant B Channel V)

ALU_MCRF Master Controt, p. 128

Registers ALU CBY, ALU CBU, and ALU CBV specify the constant values for Operand B, based on this value of field OPBS in register ALU_MCRI. See also.

-	:	1	2 .	-	-	CON	١	8 –		CON		٠
_1		7	-	-	•			, : 	. : —	_	_	:

Access Reset Description

15.9	Pvw	8	RSVD	ASVD Reserved (read as 0)
	3	£	IAG	S Com
7.0		70 FVW OH CON Co	CON	Constant Specifies the constant 8 hit value to use in place of the real
				time input stream channel for operand (9 (0 f f h)

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4.3.5.7 ALU CCR: Constant C

MANTERS HILL RDT CONSTANT C. Channel Y)
2904 (ALLI CCIX Constant C. Channel I)
2904 (ALLI CCIX Constant C. Channel II)
2907 (ALLI CCV Constant C. Channel V)

ALU MCHI Master Control, p. 128

Registers ALU CCY, ALU CCU, and ALU CCV specify the constant values for Operand C, based on the value of held OPCS in register ALU MCRI

	100			
	g	-	`	_
1	2	:	•	
:			2	
	ē		=	
1	ASVO	:	2	-
!		_	=	
		_	<u> </u>	į
į		į:	2	ļ

Access Roset Description

RSVD Heserved (read as 0)	6 RVW On 1AG Tag Specifies the constant tag be to insert or the input stream (0.1h)	10 RVW On CON Constant Specifies the constant 8 bit value to use in clace of the real.	time input stream channel for operand C (0 FFh)
Hesen	lag Sp	Constar	due aut
RSVD	140	₹	
ŧ	٤	£	1
NA.	PVW G	5	
159	•	0,	į

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4.3.6 OPU: Output Processing Unit

4.3.6.1 OPU_MCRI: Master Control

VO Address HILL RDT
2a00 (OPU, MCR1 Master Control Field 1)
2b00 (OPU, MCR2 Master Control Field 2)

Figure 3.24, OPU. Output Processor Unit, p. 68 See also: Registers OPU, MCR1 and OPU, MCR2 control the operation of the OPU for fields 1 and 2

FPS	2	ZE			Over
s:	=	2	2	2	1 2 6 5 6 1 5 1
811 ¢	Acc		Access Reset	Description	notion
ž.	RVW		0	FPS	Feed Polanty Select Controls the polanty of the held ID signal supplied to the Window Cypping subunit o Normal polanty invertigation.
=	P.			2	Interiace Mode. Specifies the input stream as interlaced or non inter- laced data
2	8			32	<u> </u>
12:4	P.		£	RSVD	Reserved (read as 0)
30	P.W.		0000	<u>.</u>	Input Data Format Specifies the format of the input data stream 0000 YCbCz 4 2 non-tagged data 0001 YCbCz 4 2 Lagged data 1000 RGB 5 6 non-tagged data 1000 RGB 5 5 sugged data 1001 RGB 3 5 5 montagged data 1101 RGB 3 3 2 non-tagged data

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2.

4.3.6.2 OPU_XBII: X Begin

Figure 3.24 OPU Output Processor Umit, p. 68 IV) Adhess HIU, RDT Frider 240? (CHU KRI) X Ragin Inlager Freid I) RND2 (OHU KRI? X Beyn Inrager Freid 2) See also

Registers OPU_XBH and OPU_XRI2 specify the 11 bit X begin value for lields 1 and 2.

1181	14 19 17 11 19 11 11 11 11	2 8	15 14 13 17 11 10 9 8 7 6 5 4 3 2 1 0	1 0 Partion of the	
------	--	-----	---	--------------------	--

4.3.6.3 OPU XEH: X End

IND Andress 18U RD1

2003 (OPU XFIL X End Inlegar Field 1) 2003 (OPU XFIZ X Find Inlegar Field 2)

Figure 3.24 OPU Output Processor Unit, p. 68

See also

Registers OPU XELL and OPU XEL2 specify the 11 bit X end value for fields 1 and 2

1		Ľ	•
1		[-
		[•
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		•	,
:	5	ľ	,
-		4	,
		^	
		•	
1	-	•	
		2	-
_	į	Ξ	-
	ĺ	2	-
nsvo		2	
		=	1
USO.		•	· · · · · · · · · · · · · · · · · · ·
			•

Bil # Access Resel Description

Reserved (read as 0)	Fird X Cohumininger Index Specifies the LL bit X and value (0.77Fh)
USVD	NW Oh F! End X Colo
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4.3.6.4 OPU_YBII: Y Begin

VO Address HIU_RDT Index 2a07 (OPU_YBII. Y Begin Integer Field 1) 2b07 (OPU_YBI2 Y Begin Integer Field 2)

Figure 3:24 OPU Output Processor Unit, p. 68 See also. Registers OPU_YBI1 and OPU_YBI2 specify the 11 bit Y begin value for helds 1 and 2.

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		ASVD	ę						İ	ē				1
Bit # Access Reset Description 15.11 R/W Oh RSVD Reserved (read as 0) 10.0 R/W Oh Bi Begn Y flow integer index Species the 11 bit witeger portion of the 11 bit viteger portion of the	ş	9.	12	Ξ	0.	•	-	~	•	•	_			•
Oh RSVD	100	Access	. Reset	Des	cripti	Ę	Ì				l	-		
RVW ON BI	2 =	P.	£	PSV	٥	Reserve	pe (reac	d as 0)				i		į
	0 01	PVW	ŧ	æ		Begin 1	Post	nleger value (Index 0 75 Fh	Specifies #	=	ž.	ger portio	o of the

4.3.6.5 OPU_YEN: Y End

VO Address HIU_RDT Index 2a06 (OPU_YEII: Y End Integer Field 1) 2b06 (OPU_YEI2: Y End Integer Field 2)

Figure 3:24 OPU: Output Processor Unit, p. 68 See also. Registers OPU_YEI1 and OPU_YEI2 specify the 11 bit Y end value for fields 1 and 2

		RSVO							İ			i i		i i	: •	
5	2	5	15 14 13 12 11 10 9 0 7 6 5 0 3 2	=	9						• •	•		~	-	
=	Acc		Bit # Access Reset Description	8	criptic	Ę			ļ	Ì		1		Ì	Ì	
15 11 RVW	\$		£	PS.	RSVD Reserved (read as 0)	Reservi	Eq (rea	d as 0	ed as 0)				:	:	•	
10 0 FVW	P		£	E.		End Y Row Integer Index Specifies the 11 bit Y and value (0.7f 1s)	Now In	reger	Index Specifies the 11 bit Y end value (0.7F1)	Specif	es the	=	ا ج	dvahu	9	Į.

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4.4 RFU: Reference Frame Unit — Registers

Table 4-6. RFU registers Accessed by the Register Data Port

Ref. Section		44.9	
Definition		Master Control	
fnder	MMU: Memory Management Unit	MANU MACFI 4000	
Ne ao	MMU: Memory	MANU MCR	

OSEN MED	7007		
	000	Object Buffer 0 Master Control	4 4 1 1, page 140
URIUG FIFX	4801	Object Buffer 0 Reference Frame X Size	4412, page 141
OBUG 1 St	4602	Object Buffer 0 Linear Start Address Low	4 4 1.3, page 142
OBUG LSH	4803	Object Buffer 0 Linear Start Address High	4 4.1.3, page 142
ORUe, BSX	4804	Object Buffer 0 Buffer X Size	4 4 1.4, page 143
OBU6_BSY	4805	Object Buffer 0 Ruffer Y Size	4.4.1 4, page 143
Office DEC	4606	Object Buffer 0 Decimate Control	4 4.1 5, page 144
DBU! INCR	4810	Object Buffer 1 Master Control	4411, page 140
DBU! PFX	4811	Object Buffer 1 Reference Frame X Size	4 4 1 2, page 141
DRUI LSL	4812	Object Buffer 1 Linear Start Address Low	4 4 1 3, 0309 142
OBITI LSH	4813	Object Buffer 1 Linear Start Address High	4413 page 142
ORUI BSX	4814	Object Buffer 1 Buffer X Size	4 4 1 4, page 143
CARLII PSY	4815	Object Buffer 1 Buffer Y Size	4 4 1 4, Dage 143
OBU! DEC	4016	Object Buffer 1 Decimate Control	44 1 5 0906 144
OBUZ MCR	4820	Object Buffer 2 Master Control	4 4 1 1, Dage 140
OBUZ REX	4621	Object Buffer 2 Reference Frame X Size	4 4 1 2, page 141
OBI12 LSL	4872	Object Buffer 2 Linear Start Address Low	4 4 1 3, page 142
OBUZ LSM	4823 A	Object Buffer 2 Linear Start Address High	4 4 1 3, page 142
ONU? RSX	TI §	Object Buffer 2 Buffer X Size	4 4 1 4, page 143
ORUZ BSY	4825	Object Buffer 2 Buffer Y Size	4 4 1.4, page 143
ORUZ DEC	4826	Object Buffer 2 Decimate Control	4 4 1 5, page 144
YRLI3 MCR	21 8	Object Buffer 3 Master Control	4 4 1 1, page 140
MUD HEX	2	Object Buffer 3 Neference Frame X Size	4 4 1 2, page 141
3000 LSL	48.12		

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Table 4-6. RFU registers Accessed by the Register Data Port (cort)

Nene	Index	Definition	MBI. SECTION
HS 1 CNBO	4833	Object Buller 3 Linear Start Activess High	4.4.1. page 142
ORU3 BSX	¥C8¥	Object Buffer 3 Buffer X Size	4 4 1 4, page 143
OBU3 BSY	4835	Object Buffer 3 Buffer Y Size	4 4 1 4, page 143
08U3_0EC	4836	Object Buffer 3 Decimate Control	4 4 1 5, page 144
OBU4 MCR	4840	Object Buffer 4 Master Control	4 4 1 1, page 140
OBU4_RFX	4841	Object Buffer 4 Reference Frame X Size	4 4 1 2, page 141
08U4_LSL	4842	Object Buffer 4 Linear Start Address Low	4 4 1 3, page 142
08U4_LSH	4843	Object Buffer 4 Limear Start Address High	4 4 1 3, page 142
08U4_8SX	4844	Object Buffer 4 Buffer X Size	4 4 1 4, page 143
OBUA_BSY	4645	Object Buffer 4 Buffer Y Size	4 1 4, page 143
OBUA_DEC	4646	Object Buffer 4 Decimate Control	4415, page 144
OBUS_MCR	4850	Object Buffer 5 Master Control	4 4 1 1, page 140
OBUS_RFX	4881	Object Buffer 5 Reference Frame X Size	4 4 1 2, page 141
OBUS, LSL	4652	Object Buffer & Linear Start Address Low	4 4 1 3, page 142
OBUS_LSH	4853	Object Buller 5 Linear Start Address High	4 4 1 3, page 142
OBUS_BSX	4854	Object Buffer 5 Buffer X Size	4 1 4, page 143
OBUS_BSY	4855	Object Buffer 5 Buffer Y Size	44 1 4, page 143
OBUS, DEC	4856	Object Buffer 5 Decrmate Control	4 4 1 5, page 144
OBU6_MCR	4860	Object Buffer 6 Master Control	4 4 1 1, page 140
OBU6_RFX	4865	Object Buffer 6 Reference Frame X Size	4 4 1 2, page 141
OBUS, LSL	4862	Object Buffer 6 Linear Start Address Low	4 4 1 3, page 142
OBUS LSH	4663	Object Buffer 6 Linear Start Address High	4413 page 142
OBU6_BSX	4864	Object Buffer 6 Buffer X Size	4414, page 143
OBU6_BSY	4865	Object Buffer 6 Buffer Y Size	4 4 1 4, page 143
OBUS DEC	4866	Object Buffer 6 Decimate Control	4 4 1 5, page 144
OBU? MCR	4870	Object Buffer 7 Master Control	4 4 1 1, page 140
OBU7_FIFX	1/87	Object Buffer 7 Reference Frame X Size	4412 page 141
08U/ LSL	4672	Object Buffer 71 mear Start Address Low	441 1, page 142
151	4873	Obsect Buller 2 topos Crast Actions then	4413 0300 142

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table.4.6. RFU registers Accessed by the Register Data Port (cort.)

Index 4874 4875 4876

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Ref. Section

Object Buffer 7 Decimate Control

Object Buller 7 Buller X Size Object Buffer 7 Buffer Y Size

> ANIT RSY AU. 010

MUT RSX

Display Window 0 Reference Frame X Size

Display Window 0 Display Zoom Factor

Display Window 0 Linear Start Address High Display Window 0 Linear Start Address Low

4403

WUO LSH

4404

WUO WSX

4402

WIND ISL

WIN UZF WUD BEX

WU HCR

4405 4406

WUD WSY

WUO DSX

Display Window 0 Window X Size Display Window 0 Window Y Size Display Window 0 Display X Start Display Window 0 Display Y Start

4.4 3 6, page 151

4 4.3 7, page 152

4 4 3.7, page 152

4.4.3.6, page 151

Display Window I Linear Start Address High

4413

WUI ISH

4412

JST IOM

Display Window 1 Window X Size

Display Window 1 Window Y Size Display Window I Display X Start

4415

WUI WSY

WU DSX WUI DSY WUZ DZF WU? REX

WOI WSX

4 4 3 7, page 152 4.4 3.7, page 152 4 4 3.3, page 148 4 4.3 4, page 149

4.4 3 6, page 151

4.4.3.4, page 149

Display Window 1 Reference Frame X Size Display Window I Linear Start Address Low

Display Window I Display Zoom Factor

0177

WUI DZF

WUI FIFT

4407

WUO DSY

4 4 3.1, page 146 4 4.3.2, page 147

Display Window Honzontal Control Register

Display Window Master Control

JWU: Display Window Unit

90: • 400 440

WU MCR

4 4.3, page 148

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Table 4-6. RFU registers Accessed by the Register Data Port (corr.)

Name	hdex	Definition	Ref. Section
DWUZ_DSX	4426	Display Window 2 Display X Start	4 4 3 7, Dage 152
DWU2_DSY	4427	Display Window 2 Display Y Stari	4437, page 152
DWU3_DZF	4430	Display Window 3 Display Zoom Factor	4 4 3 3, page 148
DWU3 RFX	4431	Display Window 3 Reference Frame X Sibe	4 4 3 4, page 149
DWU3_LSL	4432	Display Window 31 mear Start Address I ow	4 4 3 5, page 150
DWU3_LSH	4433	Display Window 3 Linear Start Address High	4 4 3 5, page 150
DWU3_WSX	4034	Display Window 3 Window X Size	4 4 3 6, page 151
ASM COMO	4435	Display Window 3 Window Y Size	4 4 3 6, page 151
DWUJ_DSX	4436	Display Window 3 Display X Start	4 4 3 7, page 152
DWU3_DSY	4437	Display Window 3 Display Y Start	4417 0000 163

Œ

Display Window 2 Linear Start Address High 4 4 3 5, page 150

Display Window 2 Window X Size

424

Display Window 2 Window Y Size

Display Window 2 I mear Start Address Low

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4422

181 21M

WI12 1511 WILL WSX

Display Window 2 Reference Frame X Size

Display Window 2 Display Zoom Factor

Display Window I Display Y Start

4417

4.4.3.6, page 151

4.4.1 OBU: Object Buffer Unit

4.4.1.1 OBUo_MCR: Object Buffer Master Control

FILL ROT In Andress

4800 (ORITO MCH Object Buller o Master Control)
4810 (ONLIL MCH Object Buller 1 Master Control)
4820 (ONLIZ MCH Object Buller 2 Master Control)
4830 (ONLI MCH Object Buller 3 Master Control)
4830 (ONLIS MCH Object Buller 3 Master Control)
4850 (ONLIS MCH Object Buller 3 Master Control)
4850 (ONLIS MCH Object Buller 3 Master Control)
4870 (ONLIC MCH Object Buller 3 Master Control)

See also

Figure 3.28 Object Buffer, p. 72 Figure 3.29 XV 8t f. Direction Control, p. 75

The eight identical registers OBUo, MCR control the operation of the eight object buffers.

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Access Resel Description 81.0

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Disable single sweep mode Enable single sweep mode (reset OPM to 00000 after one hetri VBI F Direction Control Specifies whether the Y address counter is un cremented or decremented after each thin (see Figure 3.22) X BL1 Direction Control Specifies whether the X address counter is in FIFO Association Specifies whether the stream written into the object cremented or decremented after each line (see Figure 3.22) buffer is to be copied to one of the output EH Os No FIFO copy
Copy object buffer to FIFO A during write
Copy object buffer to FIFO A during write
Copy object buffer to FIFO E during write
Copy object buffer to FIFO C during write
Copy object buffer to FIFO D during write BLT to decreasing memory-addresses BLT to increasing memory addresses BLT to decreasing memory addresses BLT to increasing memory addresses Single Sweep Mode Access Reset Description (cont) 8 5 5 5 6 YBUC XBOC SSM ¥ 8 0 0 ₹ ₹ ₹ ₹ 2

4.4.1.2 OBUo_RFX: Object Buffer Reference Frame X Size

HIU, ROT VO Address

4831 (OBU) FIX Object Buffer 3 Reference Frame X Size)
4841 (OBUA RFX: Object Buffer 3 Reference Frame X Size)
4851 (OBUA RFX: Object Buffer 8 Reference Frame X Size)
4861 (OBUB FIX: Object Buffer 6 Reference Frame X Size)
4871 (OBU) FIFX: Object Buffer 7 Reference Frame X Size) 4801 (OBUD, RFX, Object Buffer 0 Reference Frame X Size) 4811 (OBUT, RFX, Object Buffer 1 Reference Frame X Size) 4821 (OBUZ_RFX: Object Buffer 2 Reference Frame X Size)

Figure 3-26. Object Buffer, p. 72 See also: The eight identical registers OBUG, RFX specify, for each of the eight object buffers, the 11 hit width repress) of the reference frame contenting the object buffer.

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Bit # Access Reset Description

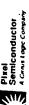
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-	Reference Frame X size (0 71 First	4
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RSVD Reserved (read as 0)	RFX Reference Frame X	i
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4.4.1.3 OBUO LSb: Object Buffer Linear Start Address

INU RUI In Address

4802 (ORINo 1S) Others thater 0 tensar Start Address Low)
4812 (ORIN1 1S) Others thater 1 linear Start Address Low)
4822 (ORIN1 1S) Others thater 2 linear Start Address Low)
4822 (ORIN1 1S) Others thater 2 linear Start Address Low)
4822 (ORIN1 1S) Others thater 3 linear Start Address Low)
4822 (ORIN 1S) OTHER THATER START Address Low)
4822 (ORIN 1S) OTHER THATER START Address Low)
4822 (ORIN 1S) OTHER START START Address Low)

4823 (OBUZ LSH Object Buffer 2 Innear Start Address High)
4823 (OBUZ LSH Object Buffer 3 Linear Start Address High)
4823 (OBUZ LSH Object Buffer 4 Linear Start Address High)
4853 (OBUS LSH Object Buffer 5 Linear Start Address High)
4853 (OBUS LSH Object Buffer 6 Linear Start Address High)
4853 (OBUZ LSH Object Buffer 8 Linear Start Address High) 4803 (ORUo 1SH Object Buffer 0 Linear Start Address High) 4813 (OBU1 1SH Object Buffer 1 Linear Start Address High)

Figure 3.28 Object Buffer, p. 72

Registers OBUO LSL and OBUO LSH specify the 23 bit linear starting address of the object buffer.

Object Butter Linear Start Address Low

Bits 15 through 0 of register UBUo LSt, specify the lower 16 bits of the 23 bit linear address.

15 | 14 | 13 | 17 | 10 | 9 | 9 | 9 | 7 | 6 | 5 | 4 | 3 | 2

Access Reset Description

Linear Start Address Low Specifies the lower bits of the 23 bit linear 0 (SB Linear Start Address (LSB must = 0) starting address (0-7FFFh) 15 ફ MAI

Object Buller Linear Start Address High

Bits 5 through 0 of register OBUo_LSH specify the upper 6 bits of the 22 bit linear address.

Access Reset Description

I mear Start Address thigh Specifies the upper 7 bits of the 23-bit hinear starting address (0.7Fh) FISVI) Hisewed (read as 0) RSVID 1 12 11 11 5 ٤ 3 3 ?

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4.4.1.4 OBUo BSa: Object Buffer Size

VO Address HIU RD1 Index 4804 (OBU0 BSX Object Buffer 0 Buffer X Size) 4814 (OBU1 BSX Object Buffer 1 Buffer X Size) 4824 (OBUZ BSX Object Buffer 2 Buffer X Size) 4834 (OBU3 BSX Object Buffer 3 Buffer X Size)

4854 (OBUS BSX Object Buffer S Buffer X Size) 4864 (OBUS BSX Object Buffer 6 Buffer X Size) 4874 (OBUZ BSX Object Buffer 7 Buffer X Size) 4844 (OBU4 BSX Object Buffer 4 Buffer X Size)

4805 (OBUo_BSY_Object Buffer 0 Buffer Y Size)

4815 (OBUT BSY Object Buffer 1 Buffer Y Size)
4825 (OBUZ, BSY Object Buffer 3 Buffer Y Size)
4835 (OBUZ, BSY Object Buffer 3 Buffer Y Size)
4845 (OBUZ, BSY Object Buffer 4 Buffer Y Size)
4845 (OBUZ, BSY Object Buffer 4 Buffer Y Size)
4855 (OBUZ, BSY Object Buffer 6 Buffer Y Size)
4875 (OBUZ, BSY Object Buffer 7 Buffer Y Size)

Figure 3-28 Object Buffer, p. 72

Registers OBUo_BSX and OBUo_BSY specify the size of the object buffer.

Object Buffer X Size

The X size of the Object Buffer is its width in pixels. The hardware always forces the LSB to 0

Access Reset Description

Contract and contract of the C Buffer X Size (0.7FFn) RSVD Reserved (read as 0) BSX £ ٤ ¥ ₹

Object Buffer Y Size

The Y size of the Object Buffer is its height in pixels

Access Reset Description

Rutter Y Size (0 21 Fh) RSVD Reserved (read as 0) BSY f ક ₹ 3

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4.4.1.5 OBUO DEC: Object Buffer Decimate Control

4006 (CRITIO DEC CHART Nufler 0 Decimale Control)
4816 (CRITIO DEC Charet Nufler 1 Decimale Control)
4826 (CRITIO DEC Charet Nufler 2 Decimale Control)
4836 (CRITIO DEC Charet Nufler 3 Decimale Control)
4836 (CRITIO DEC Charet Nufler 3 Decimale Control)
4836 (CRITIO DEC Charet Nufler 5 Decimale Control)
4836 (CRITIO DEC Charet Nufler 8 Decimale Control)
4876 (CRITIO DEC Charet Nufler 8 Decimale Control) I/O Achiress HIU HD1 hydox 4806 (ODI)

Register OBUo DEC specifies the write docimation mast. Fields DM7-DM0 are mapped to each successive group of eight pixels written into the object buffer. If a bit = 0, its corresponding pixel is written; if a bit = 1, its corresponding pixel is dropped

Bil # Access Resel Description

15.8	2	£	HSVD	
		.	Z MO	Write
	32	£	DMG	Write Decimation Mask Bit 6 0 Write priet to Frame Budler 1 (Joop priet)
.	¥2	క	SMO	With Decimation Mask Bit 5 0 Write parel to Frame Builter 1 Drop parel
_ !	3	٤٠	PM0	Write Decimation Mask Bit 4 0 Write priet to Frame Buffer 1 Drop priet
_	FVW	£	CM3	Write Decimation Mask Bri 3 0 Write priet to Frame Buffer 1 Grop priet
	= ,	5	CM	Write Decreasion Mask Bit 2 0 Write priet to frame Buller 1 Grop pixel
	¥ 21	£	DM:	Write Decimation Mask Bit 1 0 Write pred to Frame Buller 1 Drop pred

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Access Reset Description (cont.)

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Write Decimation Mask Its 0

Write pixel to Frame Buller

1 Drop pixel OMO

4.4.2 MMU: Memory Management Unit

4.4.2.1 MMU_MCR: Master Control

VO Address HIU_RDT Index 4000

Register MMU_MCR specifies the characteristics of the Frame Buffer used by the CL PX2070

			ASVD	٥					CH.		-	7 9 C	18 C	
2	13	2	2			-	•	-	•	-	~			0 !
911.6	Access	Reset	Access Reset Description	tion			-				-	-		- 1
15.5	P.	£	ASVD	RSVD Reserved (read as 0)	ea/ he	(0 se p			:			•	:	
	P.W	0	rao	Frame 0 1	Buffer (16 bm 32 bm	Frame Buffer Data Bus Width 0 16 bit wide bus 1 32 bit wide bus	ala Bus Width ide bus ide bus			•	į			
30	P.W.	0000	287	Frame 0000 0001 0010	64K 128K 128K 1 M	۳.	Config	ration		į			**************************************	•

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4.4.3 DWU: Display Window Unit

4.4.3.1 DWU_MCR: Display Window Master Control

IN Address HIU RUT

4100 (BWU MCR Display Window Master Control)

Figure 3.30 Display Window, p. 77 See also Register DWU MCR controls the operation of the display window and indicates to the RFU whether or not the CL PX2080 is present.

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	WC0		0]
	WC3 WC2 WC1 WC0		-	
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	OCC BMS		•	
	CIGP OCC MAS		6 0	
	CHISP GRP OCC IMS		6 01 :-	
F	GVSP GHSP GBP OCC MAS		12 11 10 9 6	
	GFM GVSP GHSP GBP OCC MS		13 12 11 10 9 0	
the second control of the second control to	GFP GFM GVSP GHSP GBP OCC MAS		14 13 12 11 10 9 8	
and the second of the second o	GCS GFP GFM GVSP GHSP GRP OCC BMS		15 14 13 12 11 10 9 0	· · · · · · · · · · · · · · · · · · ·

Description	
Resot	
Access	
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5	P.	•	SOO	Graphics Clock Select 0 1/24 GPC1K 1 14 GPC1K
•	FW	0	GF P	Graphics Find Polanty O normal polanty I inverted polanty
_	NA NA	0	SMI	Graphics Feed Mode 0 held polarity determined by value of GHSP on falling GVSP 1 GHSP input used as held select
~	W.		CVSP	Graphics Sync Polarity 0 active how 1 active high
! -	32		GHSP	Graphics Hypre Polarity 0 active high 1 active high
0	P.W.	0	Ē	Graphus Blank Polanty 0 active low 1 active high
!	₩.	! ! •	230	Occuded Window Control Specifies whether the present hardware configuration includes the CI PX2080 to CI PX2080 is present — system supports occluded windows in CI PX2080 is not present — system does not support occlude ad windows.
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Window 2 Control

0 Disable window Disable window Enable window Disable window Disable window Enable window Finable window Enable window Window 0 Control Window 1 Control Window 3 Control Access Reset Description (cont.) WC3 ₩C2 Š ¥Ċ 0 0 0 0 ₹ ₹ **₹** ₹

4.4.3.2 DWU_HCR: Display Window Horizonial Control Register

VO Address HIU RDT

4101 (DWU_HCR: Display Window Horizontal Control Register)

Figure 3:30 Display Window, p. 77 DWU Display Window Unit, p. 76 See also.

Register DWU, HCR shares two functions, depending on whether or not the CL PX2070 is operating with the CL PX2080, as specified by Bit OCC of register DWU_MCR.

When Bit OCC of register DWU, MCR = 0, the CL PX2070 is operating with the CL PX2080, and DWU_MCR specifies the number of pixel periods in the horizontal line active interval for the output CR1 Horizontal Active Count

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Bit # Access Reset Description

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interface Mode Select. Specifies whether the stream stored in the object buffer for display by the current display window is interfaced or non-

Progressive video (non interfaced) Interfaced video

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Reserved (read as 0)

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C1.-PX2070 Video Processor

Video Processor CL-PX2070

4.31 4.31 F. C. C. 1.37 F.

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9	3
4.4.3.4 DWUd_RFX: Display Window Reference Frame X Size	;
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٥	\$5
3	VO Address HIU_RDT
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₩.	Z
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	_
4	_

when Bit OCC of register UWU, MCII. - 1, the CL PX2070 is not operating with the CL PX2080, and UWU. HCR specifies the minimizm number of pixel periods required to soparate display windows.

.

'n

•

RSVD

Access Reset Description

Minmum Window Separation (0:ffh)

MWS

₹ ₹

HSV() Reserved (read as 0)

£ £ 4.4.3.3 DWUM DZF: Display Window Display Zoom Factor

440 (DWUO RFX: Display Window o Reference Frame X Size)
441 (DWU) RFX: Display Window I Relievence Frame X Size)
442 (DWU) RFX: Display Window 2 Relievence Frame X Size)
4431 (DWU) RFX: Display Window 3 Relievence Frame X Size) Index

Figure 3.30 Display Window, p. 77

Register DWUd_RFX specifies the 11 bit pixel width of the reference frame containing the display wire

-		-		
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RFX		١	~	ı
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	Bit & Access Reset Description	Reset	Descrip	Sescription	
15:11	15:11 RVW	£	RSVD	RSVD Reserved (read as 0)	į
9	W/8 000	l	Afx	Rf X Reference Frame X size (0.71 Fh)	

4400 (DWI1 D TO Display Window 0 Display Zoom Factor)
4410 (DWI1 DE TO Display Window 1 Display Zoom Factor)
4420 (DWI1 D TO TO Display Window 2 Display Zoom Factor)
4420 (DWU2 DZ TO Display Window 3 Display Zoom Factor) HIU RDI I/O Address

Register DWUd DZF specifies the X and Y zoom factors to be applied to the display window output. Functional orly when used with CL PX2080 Specifies zoom factor. The image is scaled according to the following formula.

For example, a zoom factor of 128 yields a scaling factor of 2. A scaling factor of one (no change in image Scaling . JOHNS LACTOR size) is selected by entering a zoom factor of zero.

NOTE: The contents of the object buffer are not affected by the zoom factors.

		•
acital and a second		

YZOOM Y Zoom Factor — fine rephcation value (0 FFh)	RVW Oh X200M x 200m Factor – pixel replication value (0 F ft)	
7. A.	x x	
R/W	P.	
15.8	. 0,	it.

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CI.-PX2070 Video Processor

r Start Address	
Start	
Linear	
DWUd_LSb: Display Window Linear	
Display	
r Sp	
DWC	
14.3.5	

HIU ND1 442 (NWIU LSL Droplay Window 0 Imear Start Address I ow) 442 (DWII LSL Droplay Window 1 Imear Start Address I ow) 442 (DWII LSL Droplay Window 2 Imear Start Address I ow) 4432 (DWUJ LSL Droplay Window 2 Imear Start Address I ow) In Address

4403 (DWIJO 15H Display Window 01 inear Start Address High)
4421 (DWILP 15H Display Window 11 Inear Start Address High)
4421 (DWILP 15H Display Window 2 Linear Start Address High)
4431 (DWUJ_15H Display Window 3 Linear Start Address High)

Figure 3.30 Display Window, p. 77 See also Register DWUd 1.St and DWUd 1.SH specify the 23 bit linear starting address of the display window.

Bits 15 through 0 of register DWUd LSL specify the lower 16 bits of the 23 bit linear address. Display Window Linear Start Address Low

1.58

Access Reset Description

Linear Start Address Low. Specifies the lower bits of the 23 bit linear) (SB Linear Start Address (LSD must - 0) starting address (0.7fffh) 3

Display Window Linear Start Address High

Bits 6 through 0 of register DWUd LSH specify the upper 7 bits of the 23 bit linear address. 7 0 6 01 11 21 61 11 12

Bit # Access Reset Description

RISVI) Reserved (read as 0)	1 SH Linear Start Address then Specifies the upper 7 bits of the 23-bit linear	starting andress (0 7Fh)	
USAD	ryw on tSir		
£	5		
15.7 RW Oh	3.5		
15.7	6.0		

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CL-PX2070

Video Processor

4.4.3.6 DWUd_WSa: Display Window Size

Semiconductor

HILL RDT VO Address

4404 (I)WIJD WSX Display Window 0 Window X Sizel 4444 (I)WUIZ WSX Display Window 1 Window X Sizel 4424 (I)WUIZ WSX Display Window 2 Window X Sizel 4424 (I)WUIZ WSX Display Window 3 Window X Sizel

4405 (DWUD, WSY Display Window 0 Window Y Size)
4415 (DWUI, WSY Display Window 1 Window Y Size)
4425 (DWUZ, WSY Display Window 2 Window Y Size)
443 (DWUIZ, WSY Display Window 3 Window Y Size)

Figure 3-30 Display Window, p. 77

Registers DWUd_WSX and DWUd_WSY specify the size of the display window.

Display Window X Size

Register DWUd_WSX specifies the X dimension of the display window in pixels

HSVD WSX 15 11 10 9 6 7 6 5 4 3 7 7 1		٠ ـ
6 01 11 21		٥
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6 01 11 21		-:
6 01 11 21		_
6 01 11 21		~
6 01 11 21		
6 01 11 21		-
6 01 11 21		
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6 01 11 21		\vdash
ASVD 15 14 10 9		
15 14 13 12 11 10 9		<u>Ц</u>
ASVD 15 14 10 10		
ASVD 15 14 13 12 11 10		الل
ASVO 15 11 11 11 11		
ASVD 12 14 13 12 11		=
15 14 13 12 11	_	
15 14 13 12		=
15 14 13 12		\vdash
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15 14 13	_	\vdash
\$1 \$4	2	2
15	č	Ш
ž		-
ā		-
لسخب		=
	_	

Access Reset Description

_	15 11	P/W	ъ	RSVD	Reserved (read as 0)	
	100	₹	£	WSX	(Window X Size (LSb must = 0)	
						 ť

Display Window Y Size

Register DWUd_WSY specifies the Y dimension of the display window in pixels

		0	•
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L		_	ر

Description Access Reset

15 11	3	£	ASVD	111 RVW On RSVD Reserved (read as 0)
100	P,W	٤	WSV	WSY Window Y Size (0.7FFh)

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4.4.3.7 DWUd_DSa: Display Window Display Start

INU RD In Address

4406 (DW10 IBX Dictivaly Window 0 Display X Slari) 446 (DWII DSX Display Window 1 Desplay X Slari) 445 (DWII? DSX Display Window 2 Display X Slari) 4416 (DWII? DSX Display Window 3 Display X Slari)

4407 (DWUO DSY Display Window o Display Y Slani)
4427 (DWUL DSY Display Window Lipsplay Y Slani)
4427 (DWUL DSY Display Window 2 Display Y Slani)
4437 (DWU3 DSY Display Window 3 Display Y Slani)

Figure 3:30 Display Window, p. 77

Registers DWUd DSX and DWUd DSY specify the location of the top left corner of the display window retative to the top left corner of the output CRT display.

Display Window Display X Start

Register DWUJd DSX specifies the pixel offset from the CRT column 0 to the left most column of the dis-

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NSO	•
İ	~
	•
!	•
i	2
	=
	2
ASVD	15 14 13 12 11 10 9 8 7 6 5 4 3
usvo	2
	5

15 12 FWW On RSVD Haseword (read as 0)	. 3	2 8	Bit # Access Reset Description	- 8 6	criptk	٠	•	0	•	<u>-</u>	-	-	2	-	0
On OSX (hsplay X Start (0 7F fh)	•	15 12 RVW	8	NSV	9	leserve	d (read	(as 0)							
OSX	. :	i				:									П
	3		£	OSX		hsplay	X Start	7 (0)	E						

Angister UWUd_DSY specifies the pixel offset from the CRT row 0 to the top-most row of the display win-

Display Window Display Y Start

_			_
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		~	1
		-	1
		•	
-	DSV	ŀ	
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		2	į
		=	İ
		21	
	USVD	2	
	ns	15 14 13 12 11 10 9 8 7 6 5	I II I I I I I I I I I I I I
1		=	· :

Access Reset Description

15.12 RVW	<u>\$</u>	£	RSVD	RSVI) Reserved (read as 0)
	F.W	8	RVW ON DSY	Display Y Slart (0 7FTh)

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Video Processor CL-PX2070

CL-PX2070 Video Processor



5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

permanent damage to the dewice. This is a stress rating only, and functional operation of the dewice at these or any conditions above those indicated in the operational sections of this speculcation is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability. This section lists the absolute maximum ratings of the CL PX2070. Strosses above those listed can cause 65* to .150° C 0 5 Volts to V_{DD} +0 5V Voltage on any pin with respect to ground Power Supply Voltage Storage temperature

5.2 CL-PX2070 Specifications (Digital)

Lead Temperature (10 seconds)

300.C

Symbol	Parameter	Z.	MAX	Units	Conditions
QQA	Power Supply Voltage	4 75	\$ 25	>	Normal Operation
	Input Low Voltage	0	90	>	
Ŧ	Input High Voltage	20	VD0 + 08	>	:
٥	Output Low Voltage		•0	>	Ly: 4 mA
Ϋ́	Output High Voltage	24		>	less = 400 µA
00	Digital Supply Current		₹ 2	¥E	V _{DO} Normal
1001	Total Supply Current		¥	¥E	Noie 1
	Input Leakage	o.	9	٧į	O < VIN < VDD
Z	Input Capacitance		9	J.	
S	Output Capacitance		01	5	

NOTE: 1) log1 is the sum of log + DAClog + CLK(pg, and must be < 200 mA (package constraint) 2) DACVSS must not exceed V_{DD}.

5.3 CL-PX2070 DC Characteristics

(VDD = 5V 5%, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Unils	Conditions
lomas	Output Current		21	¥	V1 > 0V
S	Output Capacitance		2		Pipith - Vg MAX

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CL.-PX2070 Video Processor

NOTE: 1) to is measured from the 50% point of VIXCI K to 50% point of full scale transition 2) Load is 37 S ohms and 30 pl per analog output 3) Ing pr = 8 8 mA

4) Ig is measured from 10% to 90% full scale.

5) is is measured from 50% point of hat scale transition to output remaining within 2% of final value.

6) Outputs loaded identically

?) About the mid point of the distribution of the three DACs measured at full scale deflection

5.4 AC Characteristics/Timing Information

This soction includes system timing requirements for the CL PX2080. Timings are provided in nanoseconds (ns), at TTL input levels, with the ambient temperature varying from 0 to 70° C, and V_{CC} varying from 4.75 to 5,25V OC.

NOTE: 1 All himmags assume a load of 50 pf 2 111, signals are measured at CMOS lineshold 2 111, signals are measured at 111 timeshold. CMOS signals are measured at CMOS lineshold

5.4.1 Index of Timing Information

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Acres toge Company

5.4.2 I/O Timing (ISA Bus)

Table 5-1. I/O Timing (ISA Bus)

Symbol Parameter

Symbol	Parameter	Z	MAX	Unit
ا جـ	Selup time, valid address to IOR'/IOW' active	30		Ę
12	Delay, IOR'/IOW" active to DEN' active, IDIII change		20	: :
t)	Detay, IOR* active to data out low Z	-	75	35
•	Detay, IOR' active to data out valid	-	75	25
ış	Pulse width, IOR /IOW*	90-		ans.
اور	Delay, IOR'/IOW* inactive to DEN* inactive, DDIR change		2	
1	IOR mactive to Three State delay		202	. &
و	Address hold bine from IOR'/IOW' active	0		: &
6	Setup time, data valid to IOW* macrive	50		: 2
10	Hold Ime, IOW' inactive to data invalid	0	:	
-	Delay, IOW" inactive to next IOW" or IOR" active	80		
1,2	Setup, AEN rising edge to IOW" or IOR" active	02		Ş
	Detay, IOW* or IOR* inactive to AF.N fating edge			: 2

NOTE: AEN must be low

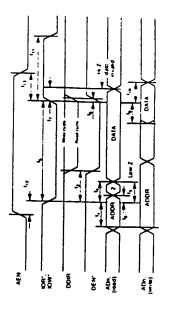


Figure 5-1. VO Timing (ISA Bus)

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5.4.3 DMA Timing (ISA Bus)

Table 5-2. DMA Timing (ISA Bus)

Symbol	Symbol Perameter	MIN	MAX	Chit
<u>.</u> -	Delay, IORY/IOW* active to DEN* active, DDIR change	•	2	2
- 2	Detay, IOR' active to data out tow Z	•	22	٤
	Detay, IOR active to data out valid		75	£
	Putse width, IORYAOW*	8		SC
			2	5 C
ا و	ION' mactive to Three State delay	-	8	ę
 ∶ <u>-</u> -	Setup time, data valid to fOW* wactive	S		£
	Hold time, IOW' inactive to data invalid			ŧ
	Delay, IOW' inactive to next IOW' or IOH' active	90		£
12	Delay, BCI K rising edge to DMARQ mactive			ns.

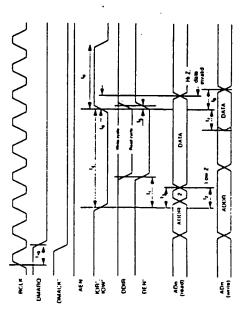


Figure 5-2. DMA Timing (ISA Bus)

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5.4.4 MCA VO Cycle Timing

Table 5-3. MCA I/O Cycle Timing

Symbol	Parameter	MIN	MAX	Ç
<u>.</u> -	Setup Imme, address valid to ADL* active	07		٤
6	Setup time, status valid to ADL' active		:	: °
9	Pulse width, ADK*	. 26	!	; ; ;
-	Hold time, status from ADL* mactive	20		. E
	Hold lime, address, MI/O' from ADI ' mactive		:	Ę
	Setup time, address valid to CMD* active	080	!	ا ا کا
,	Setup time, status vatid to CMD* active	8		S
	Setup time, ADL* active to CMD* active	35		ş
	Pulse width, CMD*	8		£
0.	Hold time, address, from CMD* active	22	<u> </u>	٤
-	Hold lime, status, from CMD* active	25		<u>ا</u> ج
2	Setup time, write data valid to CMD' active	15		Su
13	Hold time, write data valid from CMD' active	0		5
•	Detay, CMD* active to read data valid	45	1	: 2
\$	Delay, CMD' mactive to read data invalid	0	:	SE SE
9	Delay, CMD' mactive to read data high 2		30	5
,	Delay, CMD' active to DEN' active / DDIR change	:		
	Delay, CMD' mactive to DEN' mactive / DDIR change		2	. S
	Delay, CMD* mactive to CMD* active		:	. 2

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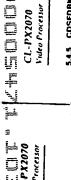
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5.4.5 CDSFDBKTIming (MCA Bus)

Table 5-4. CDSFDBK* Timing (MCA Bus)

MAX Unit	55 ns	0 os
Symbol Parameter Min	11 Address, MAO" valid to CDSFOBK detay	12 Address, MAO', invahd, CDSFDBK inactive 0

ns n NOTE: Slaves do not drive CD_S_FDBK* when they are selected by the 'Card setup' signal

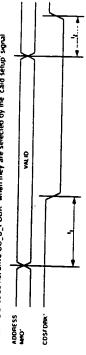


Figure 5-4. CDSFDBK* Timing (MCA Bus)

5.4.6 CDSETUP-Timing (MCA Bus)

Table 5–5. COSETUP* Timing (MCA Bus)

ن د	GLESS GO	MIN	MAX Unit	Ž.
	CMD* active to CD SETUP: inactive bold	0 8	:	٠ د د د
	ADL: mactive to CD_SETUP: mactive hold	2 2	5 5	£ . t

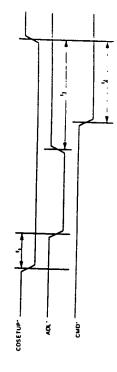


Figure 5-5. CDSETUP* Timing (MCA Bus)

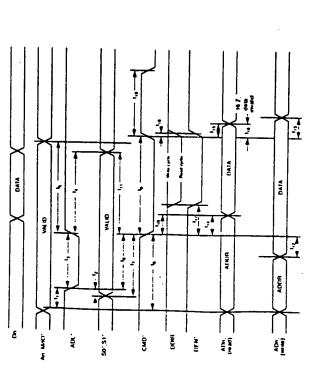


Figure 5-3. MCA VO Cycle Timing

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Table 5.-6. Local Hardware Interface Mode Wille 5.4.7 Write Timing (Local Hardware Interface)

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Symbol	Parameter	Min	MAX	Unil
ا .	period, PCI K	30		5
	pulse width, PCt K	12		\$2
بر	setup time, KOW*, CS* to PCLK rising edge	ō		Su
ا.	serup time, CS., RS[4 0] to 10W"	-		cycle
-	pulse width, 10W*	2		cycle
وا	hold time, PCLK rising edge to IOW*, CS*	2		2
- 4	delay, IOW' mactive to IOW' or IOFF active	~		cycles
ا ا و :	setup time, DATA valid to fOW mactive	15		Ş
و	hold time, CS., ftS[4 0], DATA valid to IOW" inactive	2		ε
91	delay, PCI K rising edge to READY" active	-	20	£
	delay, IOW' mactive to NFAINY' mactive	-	20	SE.
1.0	pulse width, READY*	-	2	cycles
ء !	delay, IOW active to READY active	-	-	cycle

NOTE: 1) CS', (OW', RSJ4 0) must be assened
2) II NOW' erceeds 2 cycles. Ht-AtyY is negated after 2 cycles in this case, I₁₁ is referenced to CLK.

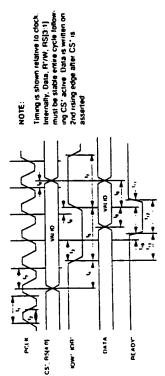


Figure 5-6. Write Timing (Local Hardware Interface)

5.4.8 Read Timing (Local Hardware Interface) Table 5~7. Local Hardware Interface Mode Read

<u>د</u> د د				
-	period, PCI K	9		£
<u> </u>	pulse width, PCLK	2.	! !	. દ
	setup time, IOH', CS' active to CLK rising edge	12	i :	: : £
و	setup time, CS', RS[4 0] valid to IOR' active	: ! -	:	Cycle
35	pulse width, IOR*	9		cycles
عد ا	hold time, PCLK rising edge to IOR' inactive, CS' mactive	2		2
	delay, fOR* inactive to IOR* or IOW* active	~	:	cycles
و	detay, IOR* active to DATA tow impedance	•	۶	٤
	detay, IOR' active to DATA valid	-	0	5
01	hold time, IOR" mactive to DATA, CS: RS[4 0] invalid	2		٤
1.5	delay, PCLK rising edge to READY' active	•		5
1.2	detay, IOR' active to REAUY' active	-	-	cycles
111	pulse width, READY*	2		Cycles
=	delay, PCLK rising edge to READY" inactive	•	2	Ş
15	delay, IOR' mactive to DATA high impedance	2	2	£

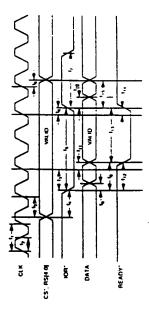


Figure 5-7, Read Timing (Local Hardware Interface)

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5.4.9 I/O DMA Timing (Local Hardware Interface)

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Table 5-8. Local Hardware Interface Mode DMA Timing

Symbol	Parameter	N N	MAX	Unit
_	period, PCI K	!		ę
٠,	pulse width, PCI K			5
٠	setup kme, DMACK', IOR'/IOW', CS', BLAST' active to PCLK rising edge			2
•	detay, DMACK' active to CS' active			cycle
<u>.</u>	delay, CS* active to IOR' 1/OW' active			cycle
ور	delay, CS* active to IOT1/IOW* mactive			cycles
-	delay, 10f1 1/OW* active to CHINDY active			cycles
٠	delay, PCI K rising edge to CHINDY* active			٤
و	delay, PCI K rising edge to read DATA vahd			2
1,0	hold brie. PCLK rising edge to read DATA invalid. READY inactive			50
<u>.</u>	delay, PCI K rising edge to IOR'AOW', CS', IILAST', DMACK' mactive			£
2	setup time, write DATA valid to CHIELY* active			£
5	hold ime, write DATA valid to PCI.K rising edge			Ş
•	delay. PCLK using edge to REATIV* inactive			5
ž.	detay, IOH* mactive to DATA high impedance			2

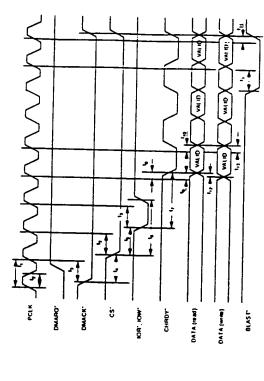


Figure 5-8. DMA Timing (Local Hardware Interface)

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Table 5-9, Input Video Timing

5.4.10 Input Video Timing

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Symbol	Symbol Parameter	MIN	MAX	MAX Unit
<u>3</u> _	phase seinp to cit	0.	,	£
£	phase hold from clk	~		73
See.	data, sync, blank valid after cits	2	5	ş
lienv	ien valid after cik	5	2	ŧ
In NS		9		٤
2	ien hold time	~		٤
	data. syncs, blank selup lime	9		S
frm:	data, syncs, blank hold time	2	 •	2

5.4.11 Input Video Timing

Table 5-10. Input Video Timing

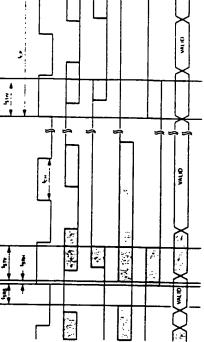
Symbol Parameter

Symbol	Parameter	MIN	MAX	MAX Unit
	minimum clock period	33		٤
	minumum clock high period	12 ns	:	20
Sns	staff request setup time	n 10	: .	ş
ISRН	staff request hold time	2		£
ISTV	staff valid after clock	/ 20 ns	2	. 5
STIV	staff invalid after clock	7 20		£

V-CLK

PHASE

¥



X 15

NA IO IN

Ved19.01

Figure 5-10, Input Video Timing

Figure 5-9. Input Video Timing

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5. PACKAGE DIMENSIONS — 160-Lead PQFP

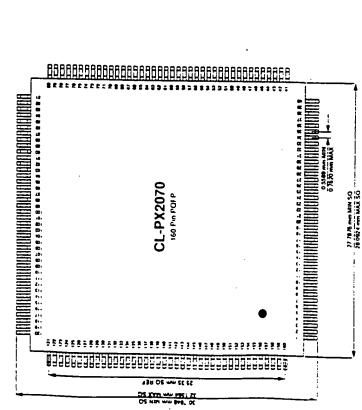


Figure 6-1, CL-PX2070 Package Information

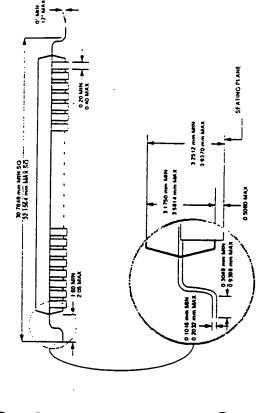
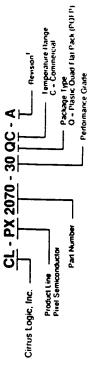


Figure 6-2, CL-PX2070 Package Information (Expanded View)

7. ORDERING INFORMATION

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